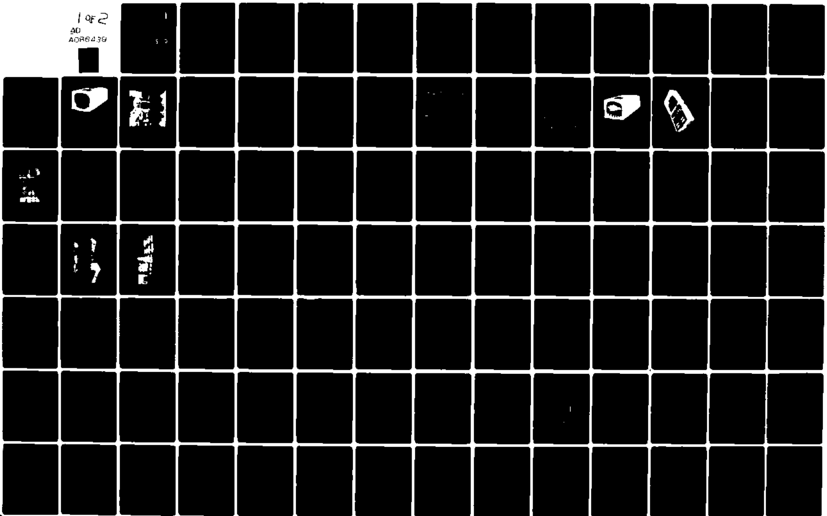
AD-A086 439 KAISER AEROSPACE AND ELECTRONICS CORP PALO ALTO CALIF F/G 17/5
DEVELOPMENT PROGRAM FOR HIGH-RELIABILITY DISPLAY IP-722 (XJ-1)A--ETC(U)
NOV 77 R MULVEY, R SWANTECK, J TISDALE N62269-75-C-0135
UNCLASSIFIED TR-77-100 NADC-75321-36 NL

1 OF 2
AD
A086439



PHOTOGRAPH THIS SHEET

ADA086439

DTIC ACCESSION NUMBER

II

LEVEL

INVENTORY

Kaiser Electronics
Palo Alto, CA
"Development Program for High-Reliability Display IP-722(XJ-1) AVA-1"
Final Engineering Rpt.
TR-77-100 NADC 75321-30
Contract No. N62269-75-C-0135
Nov. 1977

DOCUMENT IDENTIFICATION

DISTRIBUTION STATEMENT A
Approved for public release;
Distribution Unlimited

DISTRIBUTION STATEMENT

ACCESSION FOR		
NTIS	GRA&I	☒
DTIC	TAB	☐
UNANNOUNCED		☐
JUSTIFICATION		
BY		
DISTRIBUTION /		
AVAILABILITY CODES		
DIST	AVAIL AND/OR SPECIAL	
A		

DISTRIBUTION STAMP

DTIC
ELECTE
S JUL 14 1980 D
D

DATE ACCESSIONED

80 7 11 120

DATE RECEIVED IN DTIC

PHOTOGRAPH THIS SHEET AND RETURN TO DTIC-DDA-2

DTIC FORM OCT 79 70A

DOCUMENT PROCESSING SHEET

NADC 75321-30

ADA086439

UNCLASSIFIED

FINAL ENGINEERING REPORT
DEVELOPMENT PROGRAM FOR HIGH-RELIABILITY DISPLAY
IP-722(XJ-1) AVA-1

NOVEMBER 1977

PREPARED UNDER NAVAL AIR DEVELOPMENT CENTER

CONTRACT N62269-75-C-0135

FINAL REPORT TR-77-100

COVERING ACTIVITY FROM 1974 THROUGH 1977

PREPARED BY

KAISER ELECTRONICS
1651 PAGE MILL ROAD
PALO ALTO, CALIFORNIA 94306
415-493-3320

UNCLASSIFIED

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE (*When Data Entered*)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER: NADC 75321-30

2. GOVT ACCESSION NO.:

3. RECIPIENT'S CATALOG NUMBER:

4. TITLE (*and Subtitle*)
Final Engineering Report
Development Program for High-Reliability Display IP-722(XJ-1)AVA-1

5. TYPE OF REPORT & PERIOD COVERED
Final Report
1974-1977

6. PERFORMING ORG. REPORT NUMBER
TR-77-100

7. AUTHOR(s)
R. Mulvey
R. Swanteck
J. Tisdale

8. CONTRACT OR GRANT NUMBER(s)
N62269-75-C-0135

9. PERFORMING ORGANIZATION NAME AND ADDRESS
Kaiser Electronics
1651 Page Mill Road (415) 493-3320
Palo Alto, California 94306

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
S.O.W. 32591

11. CONTROLLING OFFICE NAME AND ADDRESS
Naval Air Development Center
Warminster, Pennsylvania

12. REPORT DATE
November 1977

13. NUMBER OF PAGES
160

14. MONITORING AGENCY NAME & ADDRESS (*if different from Controlling Office*)
Naval Air Development Center
Warminster, Pennsylvania

15. SECURITY CLASS. (*of this report*)
Unclassified

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (*of this Report*)
Approved for public release, distribution unlimited.

17. DISTRIBUTION STATEMENT (*of the abstract entered in Block 20, if different from Report*)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (*Continue on reverse side if necessary and identify by block number*)
Airborne video display reduces pilot workload
Supplants existing IP-722( ) AVA-1
Greater capability
FLIR display
MTBF greater than 445 hours

20. ABSTRACT (*Continue on reverse side if necessary and identify by block number*)

The IP-722( ) AVA-1 Analog Display Indicator was redesigned to provide greater reliability, new symbology, easier maintainability, built-in test capability, and FLIR video.

Four preproduction units were built in the time frame 1974-1977 and used to verify environmental performance, reliability, maintainability, and flight performance.

(Continued)

20. Some deficiencies were noted during environmental test. These deficiencies were corrected or have been analyzed in sufficient detail to permit rapid correction in the event of production go-ahead.

Reliability was demonstrated to be in excess of the specified 445 hours MTBF.

Ground and flight tests were conducted on the redesigned unit. The unit demonstrated excellent potential to provide all essential flight and attack information for the all-weather mission of the A-6E TRAM aircraft.

NADC 75321-30

UNCLASSIFIED

FINAL ENGINEERING REPORT
DEVELOPMENT PROGRAM FOR HIGH-RELIABILITY DISPLAY
IP-722(XJ-1) AVA-1

NOVEMBER 1977

PREPARED UNDER NAVAL AIR DEVELOPMENT CENTER

CONTRACT N62269-75-C-0135

FINAL REPORT TR-77-100

COVERING ACTIVITY FROM 1974 THROUGH 1977

PREPARED BY

KAISER ELECTRONICS
1651 PAGE MILL ROAD
PALO ALTO, CALIFORNIA 94306
415-493-3320

UNCLASSIFIED

ABSTRACT

The IP-722( ) AVA-1 Analog Display Indicator was redesigned to provide greater reliability, new symbology, easier maintainability, and built-in test capability.

Four preproduction units were built in the time frame 1974-1977 and used to verify environmental performance, reliability, maintainability, and flight performance.

Some deficiencies were noted during environmental test. These deficiencies were corrected or have been analyzed in sufficient detail to permit rapid correction in the event of production go-ahead.

Reliability was demonstrated to be in excess of the specified 445 hours MTBF.

Ground and flight tests were conducted on the redesigned unit. The unit demonstrated excellent potential to provide all essential flight and attack information for the all-weather mission of the A-6E TRAM aircraft.

TABLE OF CONTENTS

PART I

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF TABLES

PART I

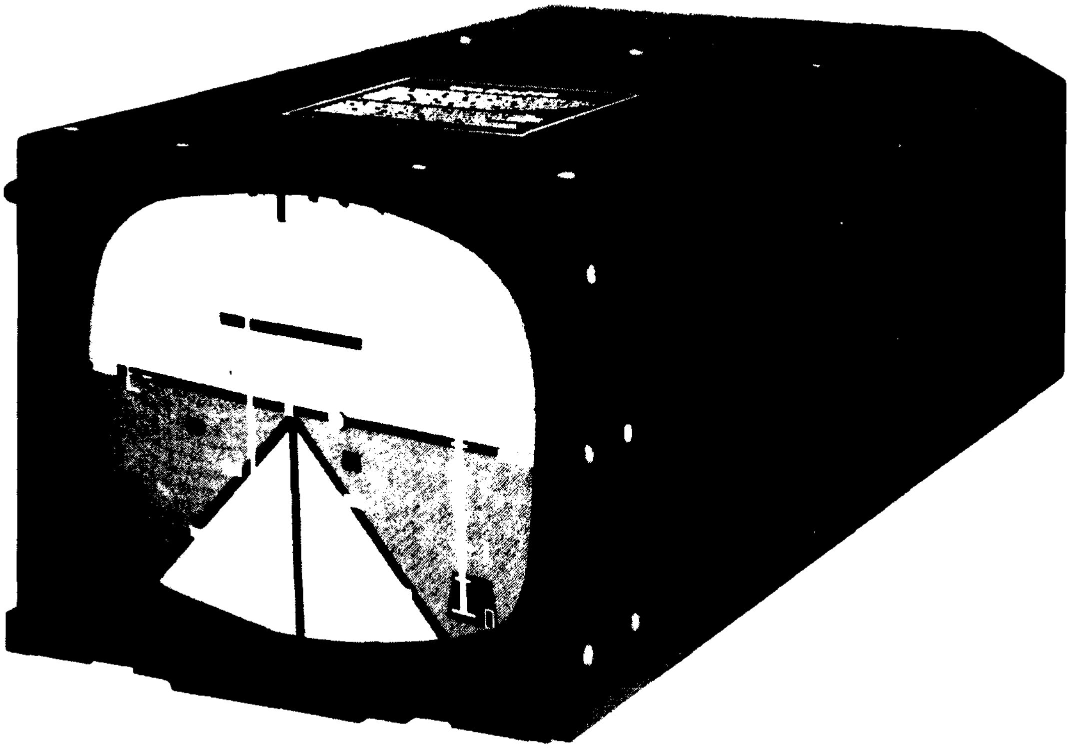
1.1 PURPOSE OF REPORT

This document is the final engineering report on the R&D contract to develop the A-6 High Reliability Display, IP-722 (XJ-1) AVA-1. The IP-722 (XJ-1) AVA-1, figures 1-1 and 1-2, is hereinafter referred to as the XJ-1.

1.2 ADMINISTRATIVE DATA

Administrative data pertinent to the contract are listed below.

CONTRACTING AGENCY:	Naval Air Development Center Warminster, Pennsylvania
CONTRACTOR:	Kaiser Electronics Corporation Palo Alto, California 94306
CONTRACT:	N62269-75-C-0135
STATEMENT OF WORK:	32591
EQUIPMENT SPECIFICATION:	DOD A013 of Statement of Work 32591
DRAWING:	Kaiser 32000 32951 Rev. 5
PART NUMBER:	Kaiser 32000-9 (Complete LRU)



STATUS: DEVELOPMENT COMPLETE

CUSTOMER: USN/NAVAIR

FEATURES:

- 525-LINE AND 875-LINE TV: VERTICAL SCAN FLIR DISPLAY AND SCAN-CONVERTED RADAR DISPLAY
- CRT SIZE 5" X 7"
- P43 PHOSPHOR WITH BANDPASS FILTER
- SYMBOL GENERATION: DIGITAL ROM & RAM TECHNOLOGY

Figure 1-1. Analog Display Indicator IP-722(XJ-1)AVA-1

3854.7

Figure 1-2. IP-722(XJ-1)AVA-1 Installed in Cockpit of A-6 Aircraft

1.3 ABBREVIATIONS

The following abbreviations are used in this report.

ACLS	Automatic Carrier Landing System
AD	Analog-to-Digital
ADC	Analog-to-Digital Converter
ADI	Analog Display Indicator IP-722( ) AVA-1
AGC	Automatic Gain Control
ALS	Short for ACLS
AOA	Angle of Attack
BAGS	Bullpup Automatic Guidance System
BIT	Built-In Test
BOT	Brief Operational Test
CA	Contact Analog
CER	Component Evaluation Report
CHL	Command Heading Lines
CRT	Cathode Ray Tube
DA	Digital-to-Analog
DAC	Digital-to-Analog Converter
DRS	Detecting & Ranging Set
EMI	Electromagnetic Interference
ETM	Elapsed Time Meter
FLIR	Forward-Looking Infrared
FSD	Field Sweep Deflection
GAC	Grumman Aerospace Corporation
HSI	Horizontal Situation Indicator
ILS	Instrument Landing System
INS	Inertial Navigation System
I/O	Input/Output
KE	Kaiser Electronics
LSB	Least-Significant Bit
LSDC	Line Scan Deflection Channel
MTBF	Mean Time Between Failures
MTBUMA	Mean Time Between Unscheduled Maintenance Action

PN	Part Number
PROM	Programmable Read-Only Memory
PWB	Printed Wiring Board
QRA	Quick-Replaceable Assembly
RAM	Random-Access Memory
RDC	Radar Data Converter
RDT	Reliability Demonstration Test
ROM	Read-Only Memory
RTV	Room-Temperature Vulcanizing (Silicone)
SACE	Shop Automatic Checkout Equipment
SDC	Synchro-to-Digital Converter
SN	Serial Number
SRA	Shop-Replaceable Assembly
TA	Terrain Avoidance
TC	Terrain Clearance
TDTA	Target Data Terrain Avoidance
TFR	Trouble & Failure Report
TM	Test Mode
TRAM	Target Recognition Attack Multisensor
VAST	Versatile Avionic Shop Tester
VDI	Vertical Display Indicator, Same as ADI
VGI	Vertical Gyro Indicator
VSI	Vertical Speed Indicator
WRA	Weapon-Replaceable Assembly
XJ-1	High-Reliability Analog Display Indicator IP-722 (XJ-1) AVA-1

1.4 PURPOSE OF DESIGN AND DEVELOPMENT ACTIVITY

The XJ-1 was designed to replace vertical display indicator (VDI) IP-722/AVA-1, first deployed in the A-6 aircraft in 1960; the VDI is described in detail in NAVAIR publication 01-85ADA-2-7.3.

With occasional minor redesign and retrofit, the VDI has remained virtually unchanged for almost 20 years. A pure analog design, the VDI uses discrete components (table 1-1), that are going out of production and becoming increasingly difficult to obtain.

Table 1-1. Parts Complement Comparison

	EXISTING VDI	NEW XJ-1
Integrated Circuits	31	443
Transistors	440	114
Diodes	513	165
Capacitors	603	345
Resistors	1424	748
Potentiometers	110	53
TOTAL	3121	1868

The purpose of the XJ-1 design and development program was to design an expanded capability display using state-of-the-art technology, digital symbol generation wherever feasible, and modular construction. Major objectives were increased reliability, easier maintainability, and one-way interchangeability with the VDI in all A-6 aircraft configurations. Additional objectives were VAST compatibility, and built-in test (BIT) capability.

Expanded capabilities were specified to be new symbology and modes as follows (figure 1-3):

- Magnetic heading scale
- Radar altitude scale
- ALS and ILS steering symbol
- Angle of attack error indication
- Incremental pitch lines
- FLIR and CONDOR video display (figure 1-4) — Condor Video Input will accept 525-line video.
- Vertical Speed Indicator

Annoyant features were eliminated by incorporating integral day and night filters and low-silhouette annunciators.

Four preproduction units were built and used to verify environmental performance, reliability, maintainability, and functional flight performance, as listed below.

SN2,SN4	Qualification Test Units
SN3	RDT Unit 1
SN4	RDT Unit 2
SN1	Flight Test Unit

A test adapter, figure 1-5, was designed to interface the existing system test set and the XJ-1.

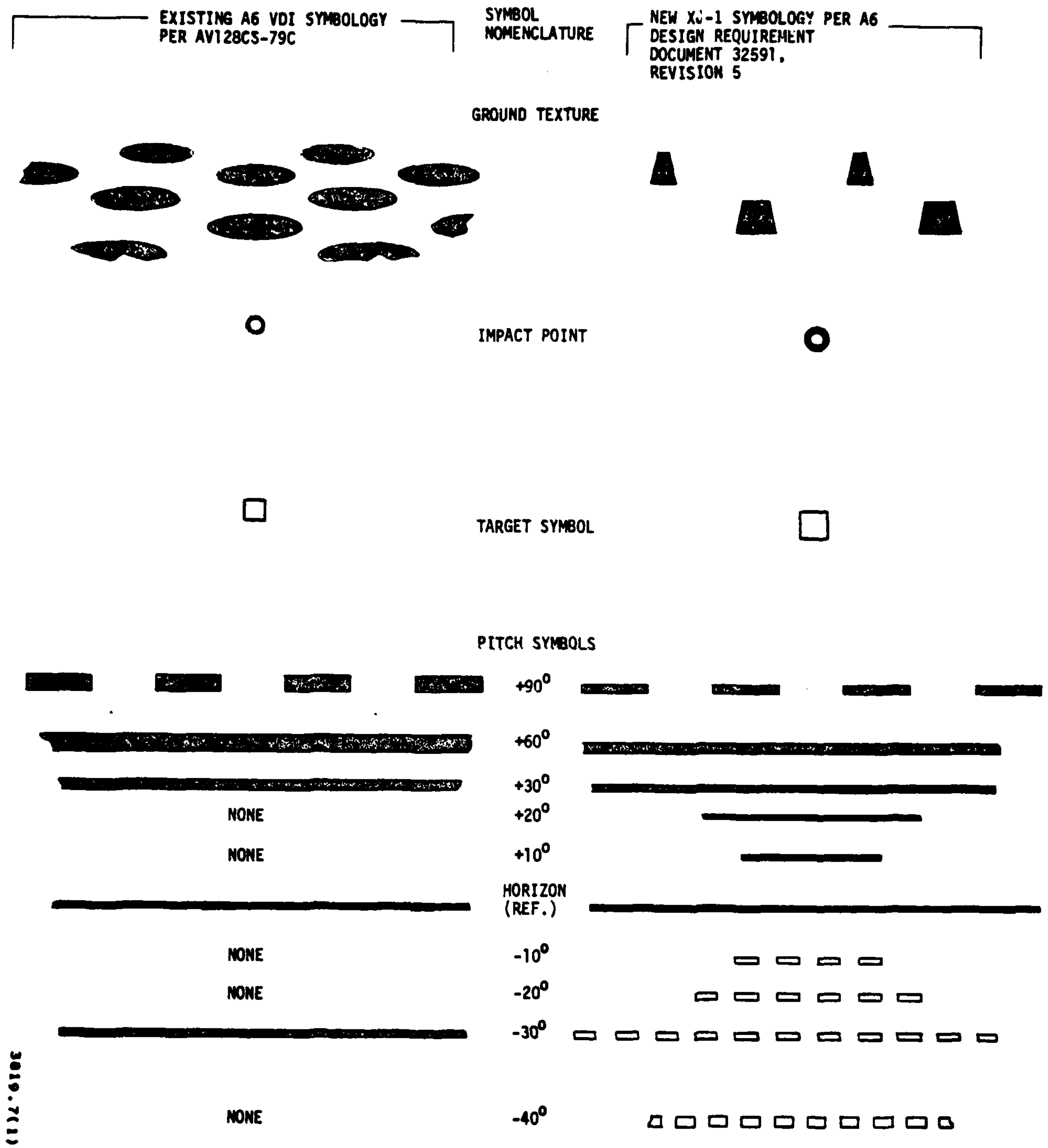


Figure 1-3. Comparison of VDI (Old) and XJ-1 (New) Symbology (Sheet 1 of 3)

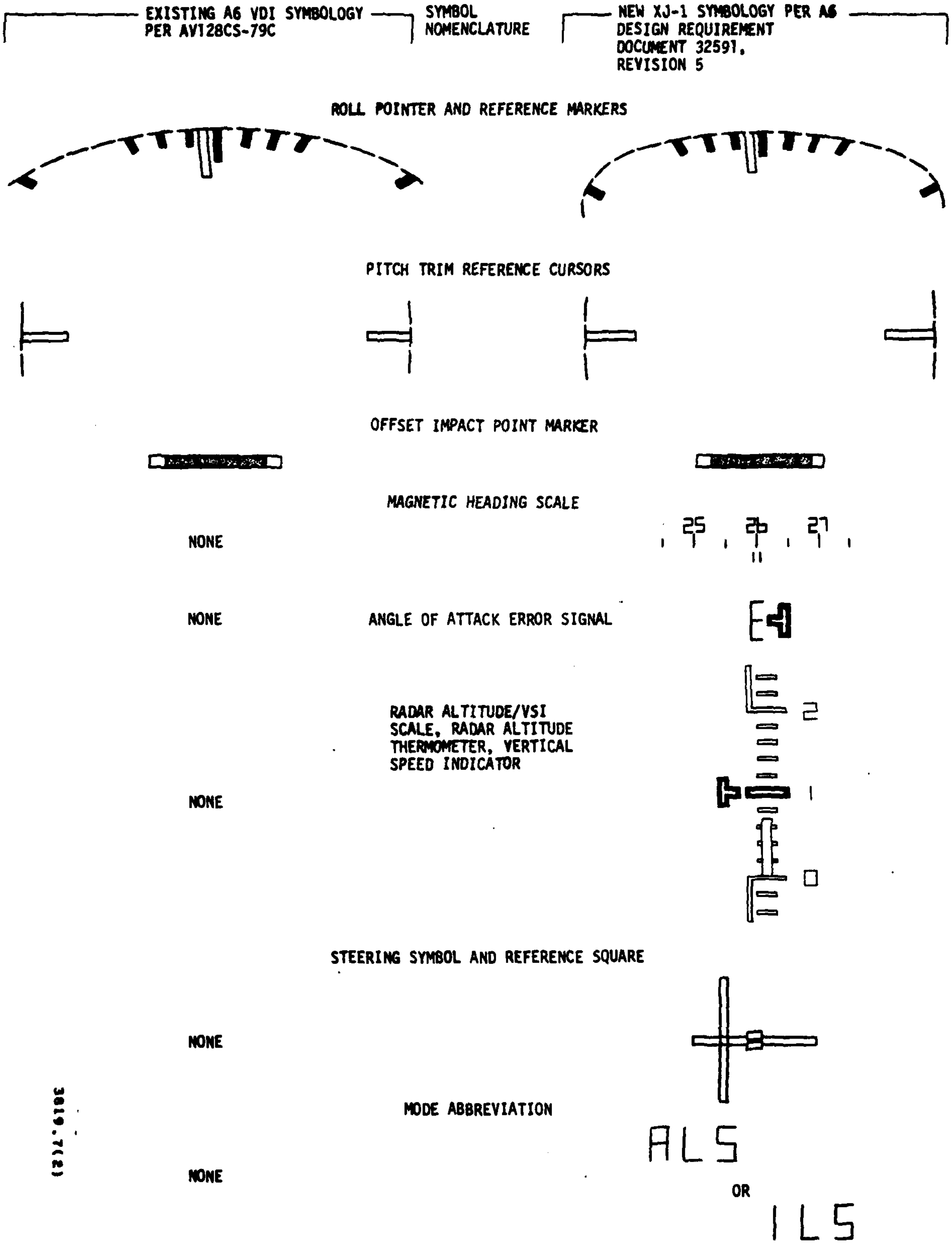


Figure 1-3. Comparison of VDI (Old) and XJ-1 (New) Symbology (Sheet 2 of 3)

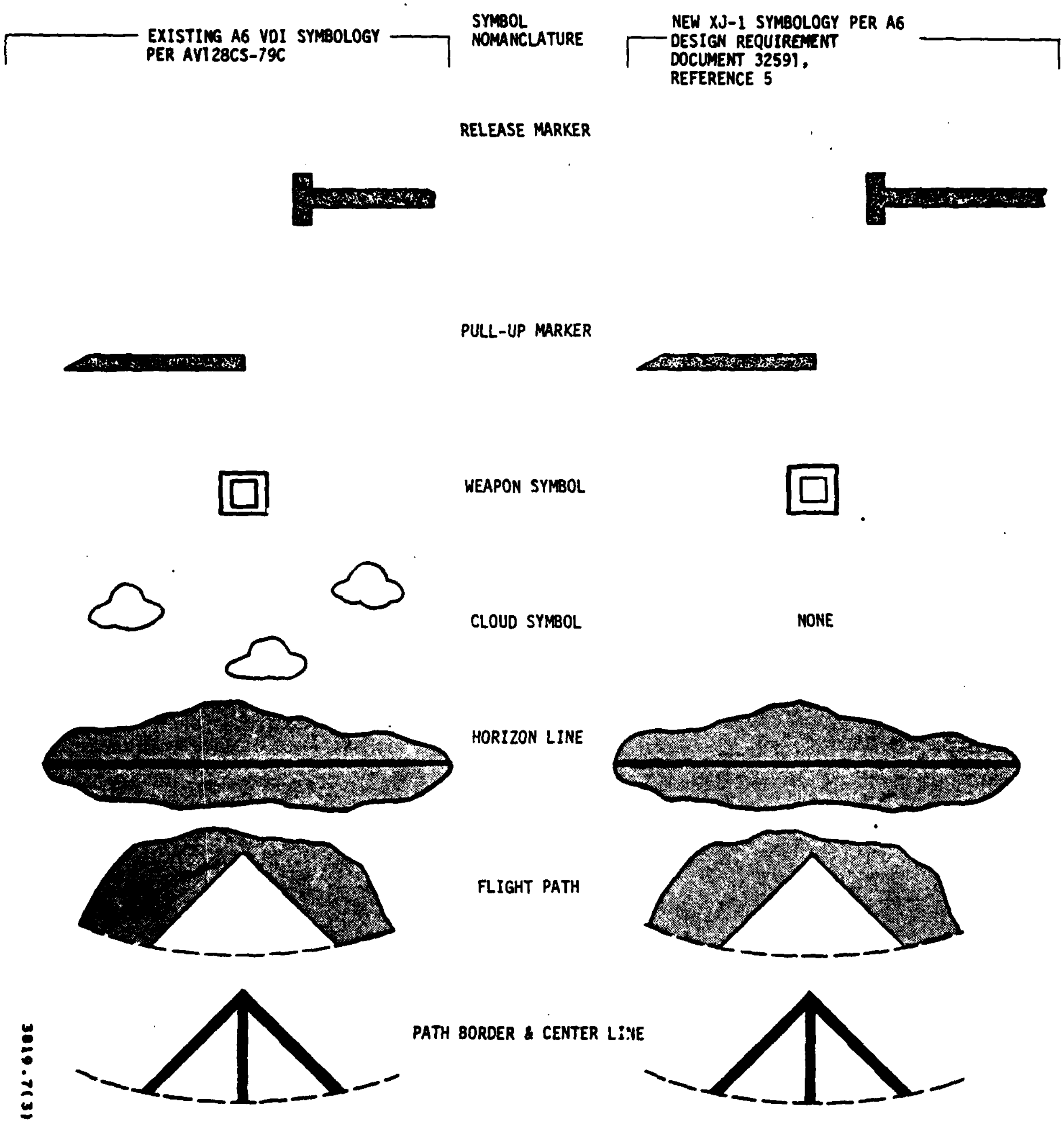


Figure 1-3. Comparison of VDI (Old) and XJ-1 (New) Symbology (Sheet 3 of 3)

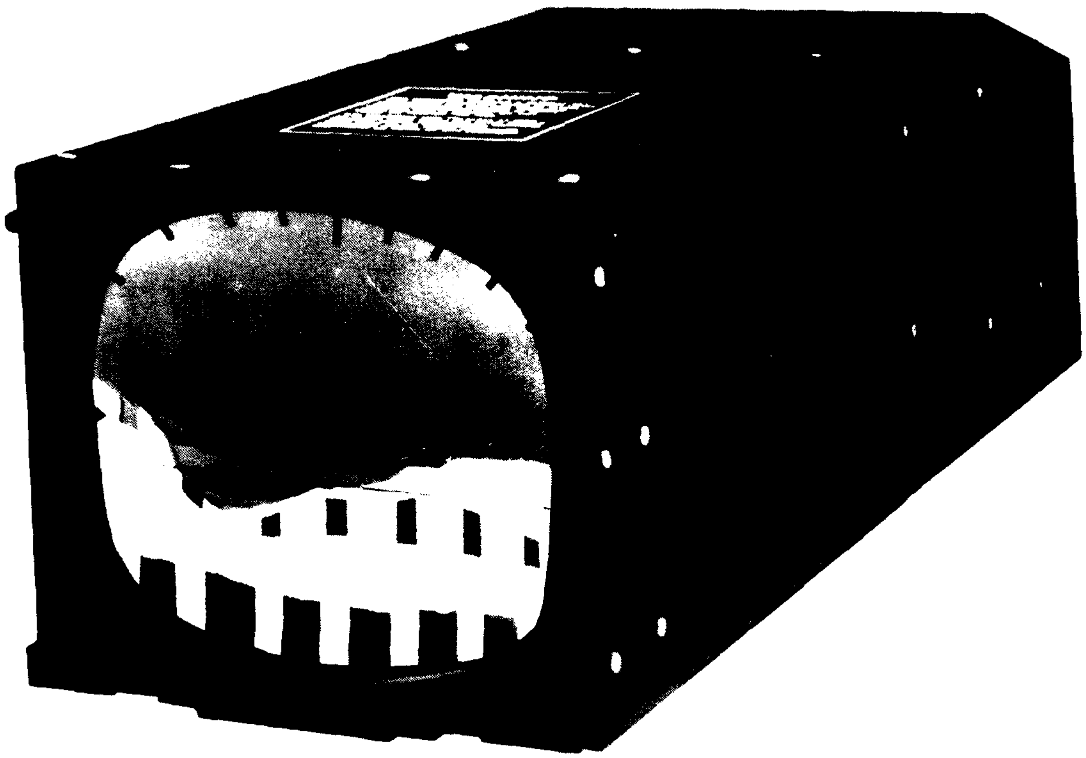
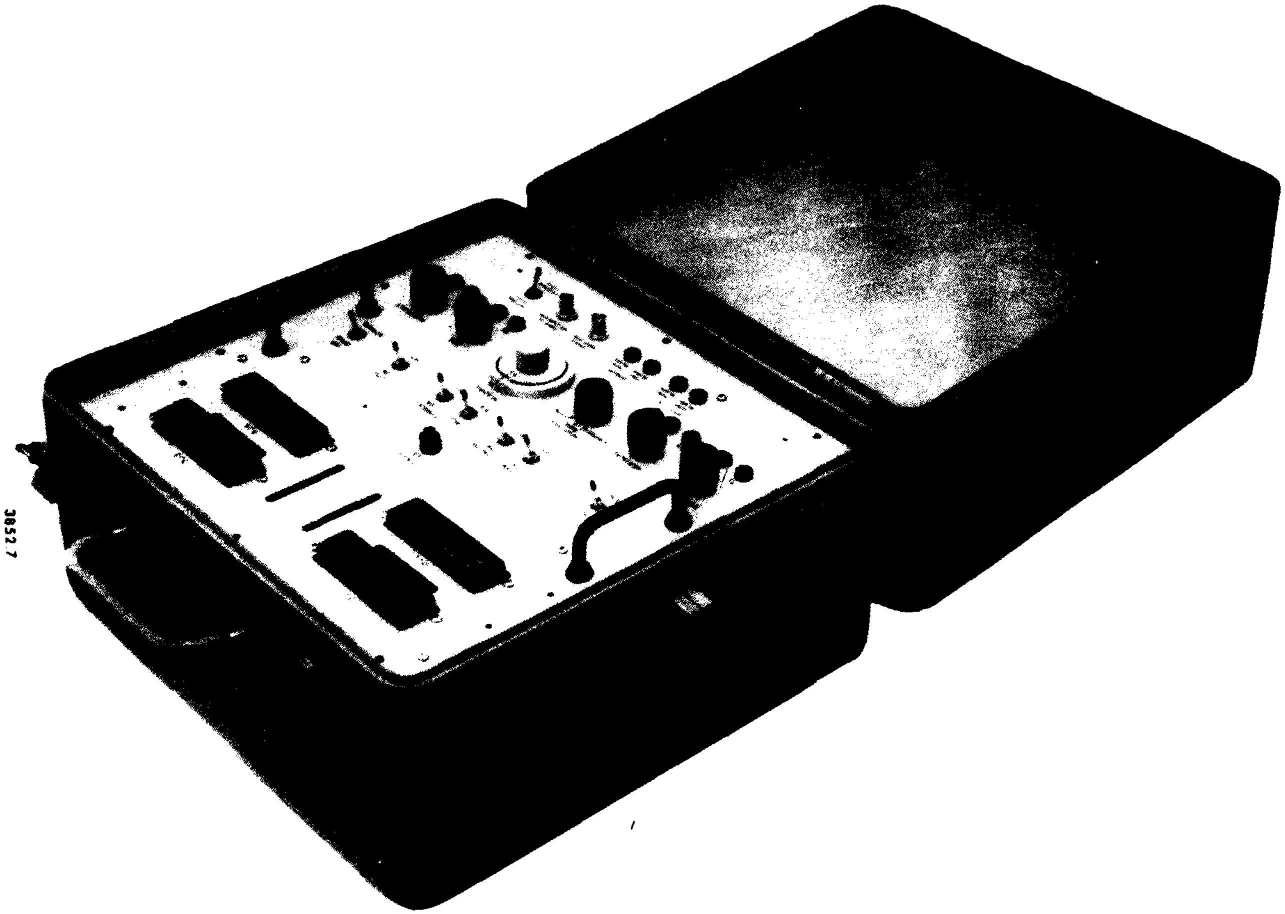


Figure 1-4. Video Display



3852 7

Figure 1-5. Test Adapter

1.5 DESCRIPTION OF EQUIPMENT

1.5.1 Overview

The XJ-1 provides the pilot with a dynamic display commonly called the contact analog mode, which electronically simulates the view seen through a forward cockpit window with a field 60^{0} in elevation and 50^{0} in azimuth. To simulate actual contact flight, the display provides a flight path presentation on a ground and sky plane as shown in figure 1-6. Symbols present information in take-off, attack, and landing modes independent of flight visibility conditions. Table 1-2 summarizes the characteristics of the various symbols.

The XJ-1 is capable of operation in terrain clearance mode, providing the pilot with a means of avoiding terrain obstacles during low-level flight.

The XJ-1 is also capable of accepting and displaying FLIR or CONDOR video in the TRAM mode.

The XJ-1 incorporates three distinct rasters for display of video and symbology in various modes. Table 1-3 summarizes the more important display parameters relating to the different modes.

Figure 1-7 through 1-13 show the physical configuration of the XJ-1 preproduction unit. Envelope dimensions and mouting requirements are identical to the VDI, as shown in figure 1-14.

The XJ-1 must operate in several aircraft models with different mode requirements. These models are:

- A6A, A6B, EA6A, EA6B, KA6D, etc. utilizing 4000-99 ADI. These models are called A6A.

- Any A6A re-wired to provide inputs from existing systems for new symbology. These models are called A6A Mod, and are identified by the presence of Aircraft Identification (Channel 114).

- A6E utilizing 4000-109 ADI

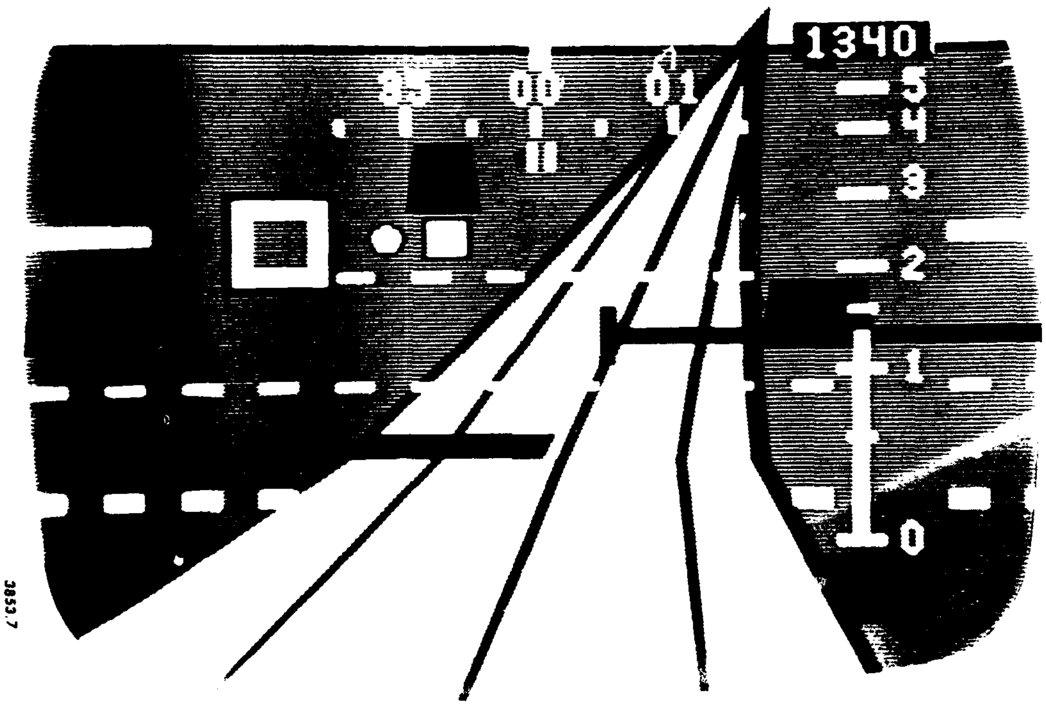
- A6E re-wired to provide inputs from existing systems for new symbology. These models are called A6E Mod, and are identified by the presence of Aircraft Identification (Channel 119).

- A6E re-wired as A6E Mod and, in addition, with TRAM systems providing high-speed line-scan FLIR. These models are called A6E TRAM II.

A limited number of aircraft are not compatible in all respects with the XJ-1. These are:

- A6C TRIM utilizing 7712-9 TRIM ADI

- A6E TRAM I utilizing 4000-119 ADI and providing 525-line FLIR video.



3853.7

Figure 1-6. Typical Display, Contact Analog Mode

Table 1-2. Symbol Description

SYMBOL/ INDICATORS	MODE	INPUT SIGNAL CHARACTERISTICS	SOURCE	REMARKS	DESCRIPTION	FUNCTION
Flight Path Border and Center Line	Contact analog Terrain clearance Test Center Line displayed in: (a) Take-off (b) Landing	Flight Path ON = +28 Vdc OFF = 0 Vdc Flight path brightness approx. equal to brightness of impact point.	Computer Control Panel		The path has black borders and center line, with a width of 1/8" ±1/16". The distance between borders and center line shall be equal.	Indicates a change in the rate of climb or dessent, and moves left or right indicating steering commands. The apex moves up, if a pull-up maneuver is required. Center line gives an indication of flight path.
Command Heading Lines	Contact analog Terrain Clearance Test Used In: (a) Attack (b) Navigation	Heading Lines ON = +28 Vdc OFF = Open	Control Panel	When not in take off or landing mode, 0 Vdc effects presence of command heading lines and removal of flight path center line.	A minimum of three dark gray lines 1/16" ± 1/32" wide, which converge above apex of flight path. Lines are spaced such that two lines enclose area equal to 1/3 that of flight path.	Command heading lines rotate in the direction of steering error.
		Horizontal Motion: -15V to +15V	Computer	Heading lines rotate about point of convergence. A +15 Vdc signal cause lines to rotate to the right at a rate of 2.63"/second. The voltage required to set lines in motion (other direction) = 0.7V.		
Flight Path Vanishing Point	Contact Analog Terrain Clearance Test	Horizontal Motion: -15V to +15V	Computer	A +15 Vdc signal moves apex 3.5" ±0.25" right of center.	Apex of flight path.	Orients both the path and command heading presentation.
		Vertical Motion: -15V to +15V	Computer	A +15 Vdc signal moves apex 1.5" ±0.25" below center of the display.		
Flight Path Near End	Contact Analog Terrain Clearance Test	Lateral Motion: -15V to +15V	Computer	A +15 Vdc signal causes center line to intersect display mask 2-1/2" ±1/4" right of center.	Widest part of flight path, located nearest the bottom of the display.	Widens or narrows with changes in altitude.
		Command Altitude Change: 0V to +15V	Computer	With the flight path vanishing point at display center, 0 to +15 Vdc shall spread the edges of the pathway near and laterally.		

Table 1-2. Symbol Description (Continued)

SYMBOL/ INDICATORS	MODE	INPUT SIGNAL CHARACTERISTICS	SOURCE	REMARKS	DESCRIPTION	FUNCTION
Flight Path Near End (Continued)				+15V (min. alt.) intersects mask 1-1/2" ±1/8" below vertical center of display. +7.5V input causes border to intersect mask 2-3/8" ±1/8" below center and 3" ±1/8" to left and right of horiz. center of display. 0 Vdc (high alt.) moves path such that edges intersect mask 1-3/4" ±1/2" to left and right of horizontal center.		
		Over-the-shoulder maneuver ON = +28 Vdc OFF = 0 Vdc	Computer and Roll Commutator Switch	Path becomes inverted and has the same size and position as above.	Provides an indication that airplane has exceeded a roll angle of $\pm(110^{0} \pm 10^{0})$.	
Pull-Up Indicators	Contact Analog Terrain Clearance Test Used In: (a) Attack	Pull-Up Marker ON = Open OFF = +28 Vdc	Computer		Black bar which extends horizontally from left flight path borderline, to within ±1/8" of path center line. Symbol grows in width from 1/8" ±1/16" to 1/4" ±1/16" as it moves downward.	Bar moves down left side of path. When the symbol reaches the bottom of screen, the command pull up is indicated.
		Distance to pull up point: -15V to +15V	Computer	The analog voltage is a function of distance to pull-up point. A +7.5 Vdc signal causes marker to move 1-15/16" ±9/32" below display center.		
		Curvature of Pull-up path: 0V to +15V	Computer	A zero signal corresponds to zero "g" or no curvature of the flight path. A +15V signal results in maximum curvature. Path edges intersect top of display mask 2-1/4" from center line of path.		

Table 1-2. Symbol Description (Continued)

SYMBOL/ INDICATORS	MODE	INPUT SIGNAL CHARACTERISTICS	SOURCE	REMARKS	DESCRIPTION	FUNCTION
Release Marker	Contact Analog Terrain Clearance Test Used In: (a) Attack	Release Marker ON = Open OFF = +28 Vdc	Computer		Black letter "T" rotated ccw. Horizontal member extends from the right of the display to within at minimum 3/4" of display center. Maximum Dimensions Horiz Member is 0.25" ±.06" wide. Vert Member is 0.75" ±12" high and 0.25" ±0.6" wide. Minimum Dimensions Horiz Member is 0.12" ±.06" wide. Vert Member is 0.38" ±.09" high and 0.12" ±.06 wide.	The symbol moves down the right side of the display, when the marker is at the bottom of the screen, weapon - release is indicated.
		Vertical Position: -15V to +15V	Computer	A +11.8 Vdc signal moves the release marker so that the horiz. member is 2.48" ±0.12" below display center. +15V places marker below display mask.		
		Marker Size: 0V to +15V	Computer	Voltage proportional to the slant or straight range to release point. 0 Vdc = minimum size. +15V = maximum size.		
Impact Pt./ Stall Symbol	Contact Analog Terrain Clearance Test	Horizontal Position: -15V to +15V	Computer ±.35	+15V places symbol 3.25" ±3/8" to left of center. 0 Vdc places symbol within ±1/8" of center.	Bright circular marker 3/16" ±1/16" in diameter. The right edge of the circle shall be outlined by a 1/16" +(1/16, -0) inch black outline.	The impact point indicates the direction of the airplane velocity vector.
		Vertical Position: -15V to +15V	Computer ±.31	+15V places symbol 2.35" ±3/8" below center. 0 Vdc places symbol within 1/8" of center.		
		Stall Signal ON = +28 Vdc	Computer	When airplane approaches stall angle of attack, symbol flashes at 2±1 Hz rate.		Stall symbol indicates stall recovery of the aircraft is required.
Weapon Symbol	Contact Analog Terrain Clearance Test	Weapon Symbol ON = Open OFF = +28 Vdc	Computer		Bright hollow square with outside dimension 0.67 ±1/16" Each leg is 1.8 ± 1/16" wide. The symbol has a 1/16" ±1/32" black outline on the right vertical edge.	Indicates direction of aim of one of the aircraft weapons.
		Weapon Symbol ON = +28 Vdc OFF = 0 Vdc	BAGS	The BAGS "on" signal is capable of overriding the computer "off" signal. Deflection circuits will also accept BAGS inputs instead of computer deflection signals.		

Table 1-2. Symbol Description (Continued)

SYMBOL/ INDICATORS	MODE	INPUT SIGNAL CHARACTERISTICS	SOURCE	REMARKS	DESCRIPTION	FUNCTION
Weapon Symbol (Continued)		Horizontal Position: -15V to +15V	Computer	A +15 Vdc signal moves the center of symbol 3.25 ±0.35" to left of display center.		
		Vertical Position: -15V to +15V	Computer	A +15 Vdc signal causes the symbol to move downward, 2.35 ±0.31" from display center.		
		BAGS Horizontal & Vertical Position: -15V to +15V	BAGS	Bull Pup guidance system has precedence over computer positioning signals. Same characteristics as above.		
Target Symbol	Contact Analog Terrain Clearance Test	Target Symbol ON = Open OFF = +28 Vdc	Computer		Bright square symbol 0.27" ±1/16". The square has a 1/16" ±1/32" black outline on the right vertical edge.	The target symbol position indicates relative target azimuth and elevation information
		Target Horizontal Position -15V to +15V	Computer	A +15 Vdc signal causes displacement of symbol 3.25 ±0.35" to left of center.		
		Target Vertical Position -15V to +15V	Computer	A +15 Vdc signal causes the symbol to move 2.35" ±0.31" below display center.		
				A 0 Vdc signal places target within ±1/8" of center.		
Pitch Trim Cursor	Contact Analog Terrain Clearance Test	Pitch Trim Cursor: ON = 0 Vdc OFF = 28 Vdc		Both pitch trim cursor and offset impact point marker are displaced vertically when offset impact pt. mk source impedance is between 0 and 10 kΩ. Only pitch trim cursor is moved for other source impedance.	Two bright cursors, extending from the display sides 3/4" ±1/4" and 1/8" ±1/16" wide.	Enable pilot to maintain a constant elevation.
		Vertical Position = 0V to +30V	Control Panel	0 Vdc places cursors 2.09" ±0.29" above horizontal center line.		

Table 1-2. Symbol Description (Continued)

SYMBOL/ INDICATORS	MODE	INPUT SIGNAL CHARACTERISTICS	SOURCE	REMARKS	DESCRIPTION	FUNCTION
Pitch Trim Cursor (Continued)				±10V places cursors within ±1/8" of nearest fiducial mk. ±20V moves cursors 2.09" ±0.29" below horiz. and +30V moves cursors below display mask.		
Pitch Lines	Contact Analog Terrain Clearance Test			The pitch lines can be superimposed upon search radar terrain clearance display.	The $+30^0$ and $+60^0$ pitch lines are black. The 60^0 line is 0.13 +0.06" 0.07 ±0.03" thick. Both lines extend across full length of display. Pitch Symbol Generators The unit generates +60, ±30, +10, and -10 pitch lines. The pitch lines shall not overlay any part of any other symbol. The $\pm30^0$ and $\pm60^0$ pitch symbols generators provide $\pm30^0$ pitch lines and $\pm60^0$ pitch line. The $+60^0$ line is 0.13 ±0.06 inch thick and the $\pm30^0$ lines are 0.07 inch ±0.03 inch thick. The $\pm30^0$ and $+60^0$ pitch lines are black and extend completely across the display. The -30^0 line consists of 0.26 ±0.06 bright segments extending completely across the screen. The spaces between segments are 0.26 ±0.06 inches in length. The $\pm10^0$ and $\pm20^0$ pitch lines are 0.07 ±0.03 inch thick, 1.8 and 2.8 inch in length, respectively, and are parallel to the horizon line.	Indicates the pitch angle of the aircraft.

Table 1-2. Symbol Description (Continued)

SYMBOL/ INDICATORS	MODE	INPUT SIGNAL CHARACTERISTICS	SOURCE	REMARKS	DESCRIPTION	FUNCTION
Pitch Trim Cursor (Continued)				±10V places cursors within ±1/8" of nearest fiducial mk. ±20V moves cursors 2-1/2" ±5/16" below horiz. and +30V moves cursors below display mask.		
Pitch Lines	Contact Analog Terrain Clearance Test			The pitch lines can be superimposed upon search radar terrain clearance display.	The $+30^0$ and $+60^0$ pitch lines are black. The 60^0 line is 1/4" ±1/16" thick. The 30^0 line is 1/8" ±1/16" thick. Both lines extend across full length of display. The $+10^0$ and $+20^0$ pitch lines are white, 1/8" ±1/16" thick, and 2.1" and 3.3" long, respectively. The $+10^0$ and $+20^0$ pitch lines are solid white lines. The -10^0 and -20^0 lines consist of four and six 0.30" ±0.06" segments respectively. Spaces are equal to segment lengths. The zenith marker ($+90^0$ pitch line) is black dashed lines of from 4 to 6 elements. Vertical dimensions are 1/4" ±1/16". Caps are the same size within ±50%.	Indicates the pitch angle of the aircraft.

Table 1-2. Symbol Description (Continued)

SYMBOL/ INDICATORS	MODE	INPUT SIGNAL CHARACTERISTICS	SOURCE	REMARKS	DESCRIPTION	FUNCTION
Pitch Lines (Cont.)					The $+10^{0}$ and $+20^{0}$ pitch lines are solid black. The -10^{0} and -20^{0} pitch lines consist of four and and six 0.26 $\pm$0.06 inch segments, respectively. Spaces are equal to segment lengths. The -40^{0} pitch line symbol generator provides a segmented bright, -40^{0} pitch line, 0.13 +0.06 inch thick. The white segments are 0.26 + 0.06 inch in length. The spaces between segments is 0.26 + 0.06. The horizon line is shaded black. The horizon line thickness is 0.07 $\pm$0.03. <u>Zenith Marker Generator</u> The zenith marker generator provides a $+90^{0}$ pitch reference. The marker is a black dashed line consisting of segments 1.0 $\pm$0.3 inches long. Each segment is rectangular and has a vertical dimension of 0.13 $\pm$0.06 inch as measured with the line located at the vertical center of the display ($+90^{0}$ pitch indication). The separation between segments is 1.0 $\pm$0.3 inch.	

Table 1-2. Symbol Description (Continued)

SYMBOL/ INDICATORS	MODE	INPUT SIGNAL CHARACTERISTICS	SOURCE	REMARKS	DESCRIPTION	FUNCTION
Horizon Line/ Ground Texture/ Sky Plane	Contact Analog Test				The horizon line is a dark tone. At zero roll, the line is parallel to the base of unit within ±0.5 degrees.	Introduce perspective into the presentation.
					Sky plane is medium gray. Ground texture consists of quasi-ransom dark trapezoids, which increase in size as they move down from horizon. Trapezoids move at 1/4" per second.	
Roll Pointer	Contact Analog Terrain Clear-ance Test	Roll Marker			A bright roll-stabilized line 1/8" ±1/16" in width. The marker extends down from the top of the screen. The end of the marker is 1.95" ±0.25" from display center.	Enables pilot to read approximate roll angles directly from display indicator.
		Reference Markers			Reference markers are dull black, located on the implosion shield, pointing toward the center of the display. The markers are spaced angularly at 0^o, $\pm 10^o$, $\pm 20^o$, $\pm 30^o$, and $\pm 60^o$. All markers are 3/32" ±1/64" wide. The 0^o ref. is 1/2" ±1/16" long, others are 1/4" ±1/16" long.	
Offset Impact Pt. Marker	Terrain Clear-ance Test	Vertical Dis-placement (a) Pitch Trim Cursor 0-30V		Vertical displacement of impact pt. symbol results in offset input pt. marker, moving (a) twice vertical distance or (b) same vertical dis-tance as the impact point.	A black rectangular horizontal bar with bright source at left and right ends. Marker length is 2" ±1/8" with a height of 0.2 ±1/8". The bright square at both	Assist the pilot in following terrain while in terrain clearance mode.

Table 1-2. Symbol Description (Continued)

SYMBOL/ INDICATORS	MODE	INPUT SIGNAL CHARACTERISTICS	SOURCE	REMARKS	DESCRIPTION	FUNCTION
Offset Impact Pt. Marker (Continued)		(b) Offset Input Pt. Marker 0-20V		Condition A - Marker manually positioned by pitch trim control and moves at same vertical rate as impact point. Condition B - Marker manually positioned by offset impact point marker and moves at the same vertical rate as impact point. With impact point set at display center and pitch trim/offset impact pt. marker adjusted between 0V and +10V, offset impact pt. marker position is .87 ±.12 below display center. When pitch trim/offset impact pt. marker is adjusted to +20V, offset impact pt. marker is 2" ±1/4" below display center.	ends of symbol are 3/16" ±1/8" in length and height.	
Angle of Attack	Contact Analog Terrain Clearance Test	Landing Mode 28V = on 0V = off		Indicates difference beween internally set angle and position of ADA probe.	An AOA reference symbol and an error symbol are provided as shown below. It consists of a fixed reference and a sidewise "T" error symbol which moves vertically about the fixed reference. The vertical deviation of the symbol represents the AOA error which is determined by the difference between an internally preset angle and the aircraft input.	Will present any error that may exist from the proper angle of attack.
Heading Scale	Contact Analog Terrain Clearance Test	3-Wire Synchro	Synchro Transmitter	Full scale = 50^{o} of azimuth 281 expanded scale.	The heading tape consists of a movable scale and associated numerics. The heading pointer serves as an index.	Indicates the present magnetic heading of the aircraft.

Table 1-2. Symbol Description (Continued)

SYMBOL/ INDICATORS	MODE	INPUT SIGNAL CHARACTERISTICS	SOURCE	REMARKS	DESCRIPTION	FUNCTION
Radar Altitude Scale	Contact Analog Terrain Clearance Test		Altimeter		Thermometer vertical scale with field indices and numerics.	Indicates both rate change of altitude and actual altitude.
ACLS Cross Pointers	Validity Signal +28 = on 0V = off Contact Analog Terrain Clearance Test	Validity Signal +28 = on 0V = off Mode 0V = ALS +28V = ILS Vertical Movements: -20 to +20V Horizontal Movements: -20 to +20V	ACLS OR ILS		Symbol consists of two independently controlled bars, one bar moving horizontally and the other vertically. Size of vertical bar: 2.0 $\pm$0.2" long .07 $\pm$0.03" wide Size of horizontal bar: 2.0 $\pm$0.2" long 0.07 $\pm$0.03" wide	Indicates vertical and lateral error of aircraft when landing on an aircraft carrier.
Inertial Subsystem Reliability Indicator	All Modes	Illuminated by +28 Vdc	Inertial Navigation System		An indicator is located at the lower left corner of the analog display panel; indicator is marked PLATFORM.	Indicator is illuminated when attitude input information has been lost, or when there is a 2° or greater lag between roll attitude signal and roll servo.
Computer Reliability Indicator		Illuminated by +28 Vdc	Computer		An indicator is located in lower right corner of the analog display. The indicator is marked COMPUTER.	Illuminates when computer information is not reliable.
Search Radar Terrain Reliability Indicator		Illuminated by +28 Vdc	Search Radar		Indicator located on the left side of the analog display panel. Indicator labeled T.C.	Illuminates when search radar information is not valid.
Altimeter Reliability Indicator		Illuminated by +28 Vdc	Radar Data Converter		Indicator located on right side of the analog display panel. Indicator labeled R.A.	Illuminates when aircraft flies below 20 feet or above 5,000 feet.

Table 1-2. Symbol Description (Continued)

SYMBOL/ INDICATORS	MODE	INPUT SIGNAL CHARACTERISTICS	SOURCE	REMARKS	DESCRIPTION	FUNCTION
In Range Indicator	All Modes	Illuminated by +28 Vdc	Computer		An indicator is located above computer indicator lamp. Indicator is marked IN-RANGE.	Illuminates when target is within minimum to maximum range of aircraft.
Attack/Laser Indicator	All Modes	Illuminated by +28 Vdc	Computer		An indicator is located above platform indicator lamp. Indicator is marked ATTACK/LASER.	Illuminates when the ballistics computer/ laser transmitter is in the attack mode.
Breakaway Indicator	All Modes	Illuminated by intermittent +28 Vdc	Computer		Two breakaway indicators, one located above T.C. indicator and one located above R.A. indicator.	Indicators will flash red color when target is within less than minimum range.
Roll Angle	CA&TC	11.3V, 400 Hz 3 phase	Inertial Navigation System. (Stator of synchro xmitter 115V, 400 Hz RS 911-6A Kear 4.44)		A synchro transformer, 11.3V, 400 Hz, R1001-1A Kearfott, accepts roll information. Unit is located in display indicator.	Delivers roll information to analog display indicator.
Elevation Angle	CA&TC	-30V to +30V	Inertial Navigation System (Potentiometer, Kaiser Spec 1733)		0V = 0^0 pitch +30V = max elevation -30V = min elevation	Delivers elevation angle information to analog display indicator.
Azimuth Angle	CA&TC	31.5 kHz variable phase	Inertial Navigation System (Resolver, Kaiser Spec PC 76010)		Variable phase input causes ground texture elements to move laterally right or left.	Delivers azimuth angle information to analog display indicator.
Ins Fail Safe	All Modes	+28 Vdc Filtered +28 Vdc Unfiltered	Inertial Navigation System		Loss of either 28 Vdc signal results in CRT blanking.	
Altitude Above Terrain Information	Terrain Clearance	Video by means of 93Ω line. Max. amplitude of 1V p-p, black negative	Radar Data Converter			Display 3-dimensional information of range, altitude, and azimuth.

Table 1-2. Symbol Description (Continued)

SYMBOL/ INDICATORS	MODE	INPUT SIGNAL CHARACTERISTICS	SOURCE	REMARKS	DESCRIPTION	FUNCTION
FLIR Composite Video	TRAM	TRAM on = 28V FLIR Video	FLIR activated at pilots control panel with TRAM on/off push-button.	Line Rate = 1488 Lines frame (44,640 Hz)	No symbols displayed.	
External Composite Video	TRAM	Condor On = 28V Discrete and TRAM ON/OFF activated	Pilots control panel	Line Rate = 525 lines/ frame (15750 Hz).	No symbols displayed.	
Sync Outputs		Horizontal: 12 μs, 5V, 15.75 kHz Vertical: 500 μs, 5V, 60 Hz	Analog Display Indicator			
Vertical Speed Indicator	TC	Input 91	Altimeter		A VSI marker and a scale are provided, comprising a sidewise "T" marker which moves vertically about the combination VSI/radar altitude scale. The vertical position of the "T" marker with respect to the fixed scale tick mark indicates +1400 ft/min, the lowest scale tick mark indicates -1400 ft/min. The zero reference for the VSI scale is the 1,000 ft tick (large 1) on the radar altitude scale and the display.	

Table 1-3. Display Parameters

1. Contact Analog Mode

- 525 line overscanned square raster with electromechanical roll
- Field sweep is from bottom to top
- Line sweep is from left to right
- 2:1 interlace, 30 Hz frame rate
- With 0^{o} aircraft roll, raster line orientation is horizontal
- 500 active lines per frame
- Vertical blanking = $\frac{25}{525}$ X(.01667 sec.) = 0.794 millisecond
- Vertical active time = 15.876 milliseconds
- Horizontal resolution = vertical resolution, thus 500 bits per active line
- Master clock frequency = 9.702 MHz
- 616 x ($\frac{1}{9702000}$) = 63.492 microseconds
- Horizontal blanking = $\frac{116}{616}$ (63.492) = 11.956 microseconds
- Horizontal active time = $\frac{580}{616}$ (63.492) = 51.536 microseconds
- Raster size = 8.33 inches x 8.33 inches
- Position resolution = $\frac{8.33}{500}$ = 0.01667 inches or $\frac{1}{60}$ inch
- Symbol size resolution = $\frac{8.33}{250}$ = 0.0333 inches or $\frac{1}{30}$ inch

2. Terrain Clearance Mode

- Identical to Contact Analog Mode

Table 1-3. Display Parameters (Cont'd)

- Horizontal sync output to RDC is advanced by 1.5 microseconds (14 bits) with respect to ADI horizontal sync (or conversely delayed by 61.992 microseconds).

  ADI Horiz Sync

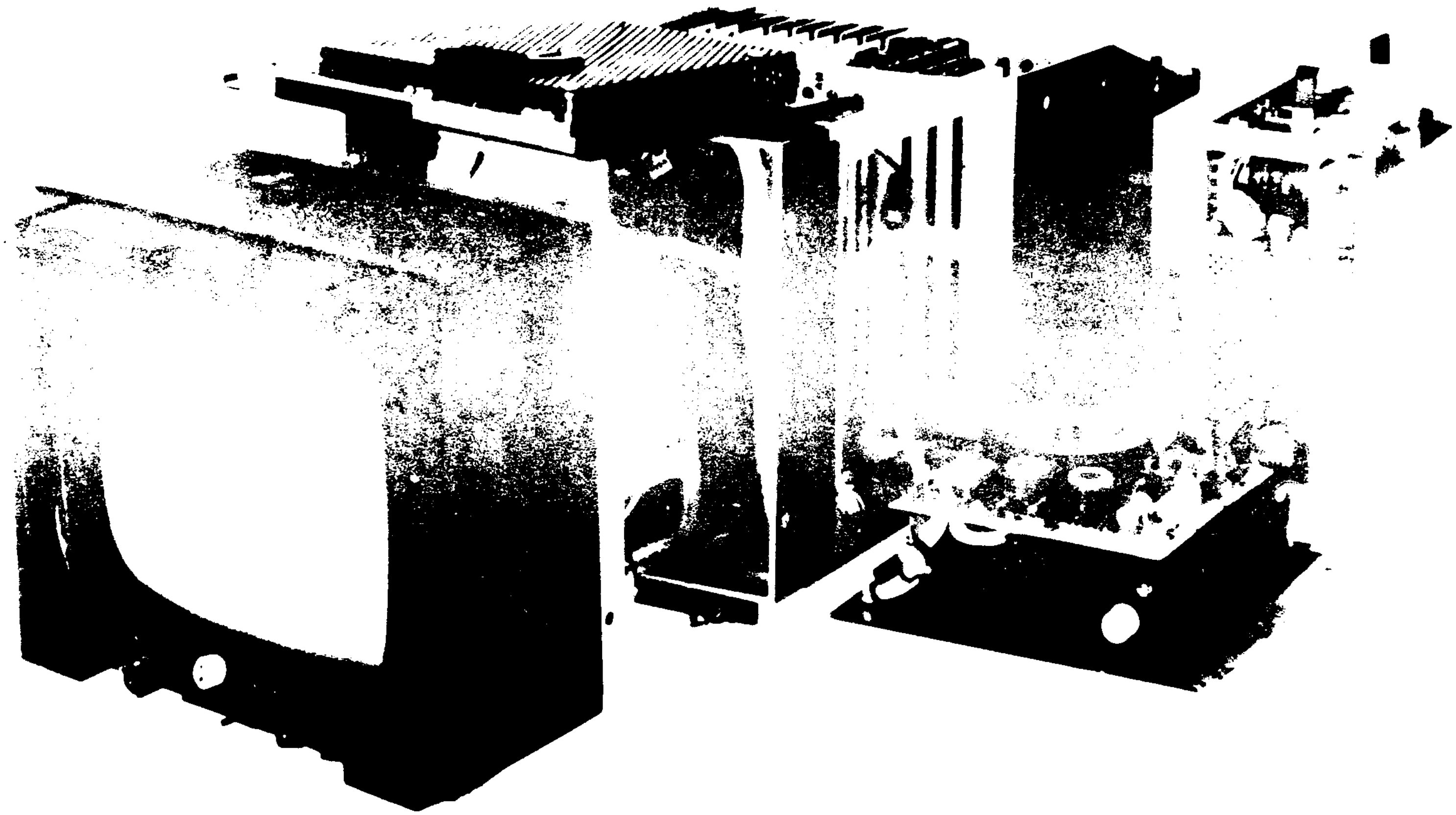
  RDC Horiz Sync

3. TRAM/Condor Mode

- 511-line stationary raster
- 2:1 interlace, 30 Hz frame rate
- Field sweep is from top to bottom
- Line sweep is from left to right
- Aspect ratio is 4h x 3v
- Raster line orientation is horizontal
- Raster size is 7.6 inches horizontal x 5.7 inches vertical
- Composite video is processed to obtain syncs
- No symbology is required

4. TRAM/FLIR Mode

- 744 line stationary raster
- Line interlace is 1:1
- Field interlace is 2:1
- Aspect ratio is 4h x 3v
- Field sweep is from left to right
- Line sweep is from top to bottom



2389.7(6)

Figure 1-7. Front View, XJ-1 Disassembled

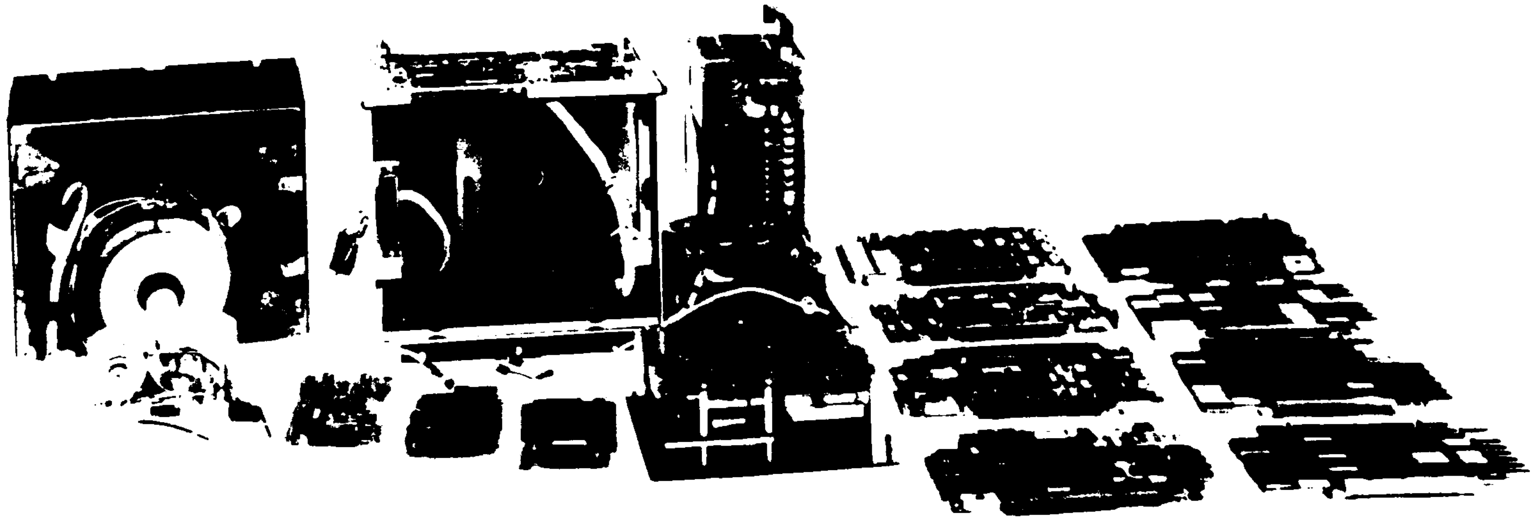


Figure 1-8. Rear View, XJ-1 Disassembled

2389.7(10)

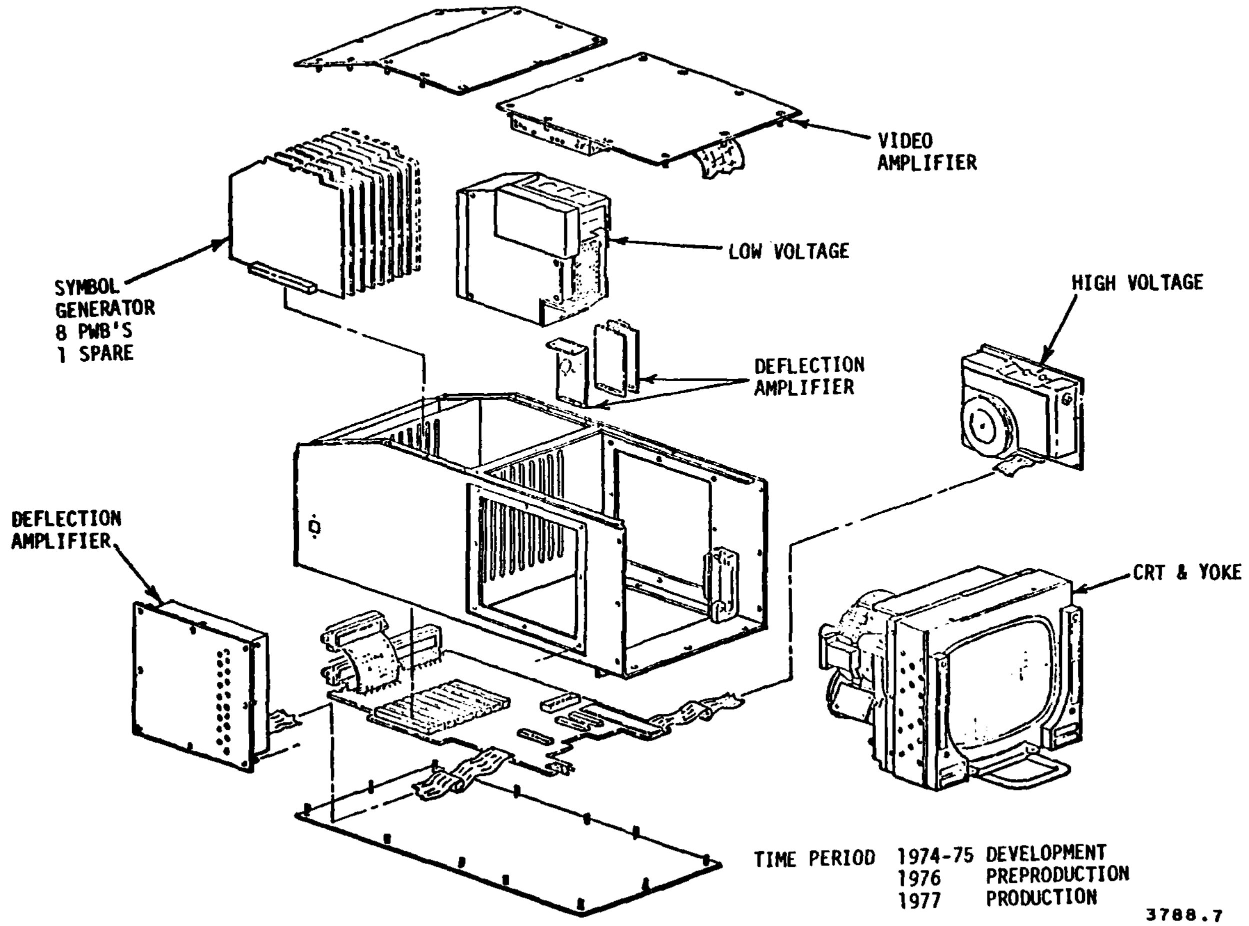


Figure 1-9. Exploded View, IP-722(XJ1) AVA-1

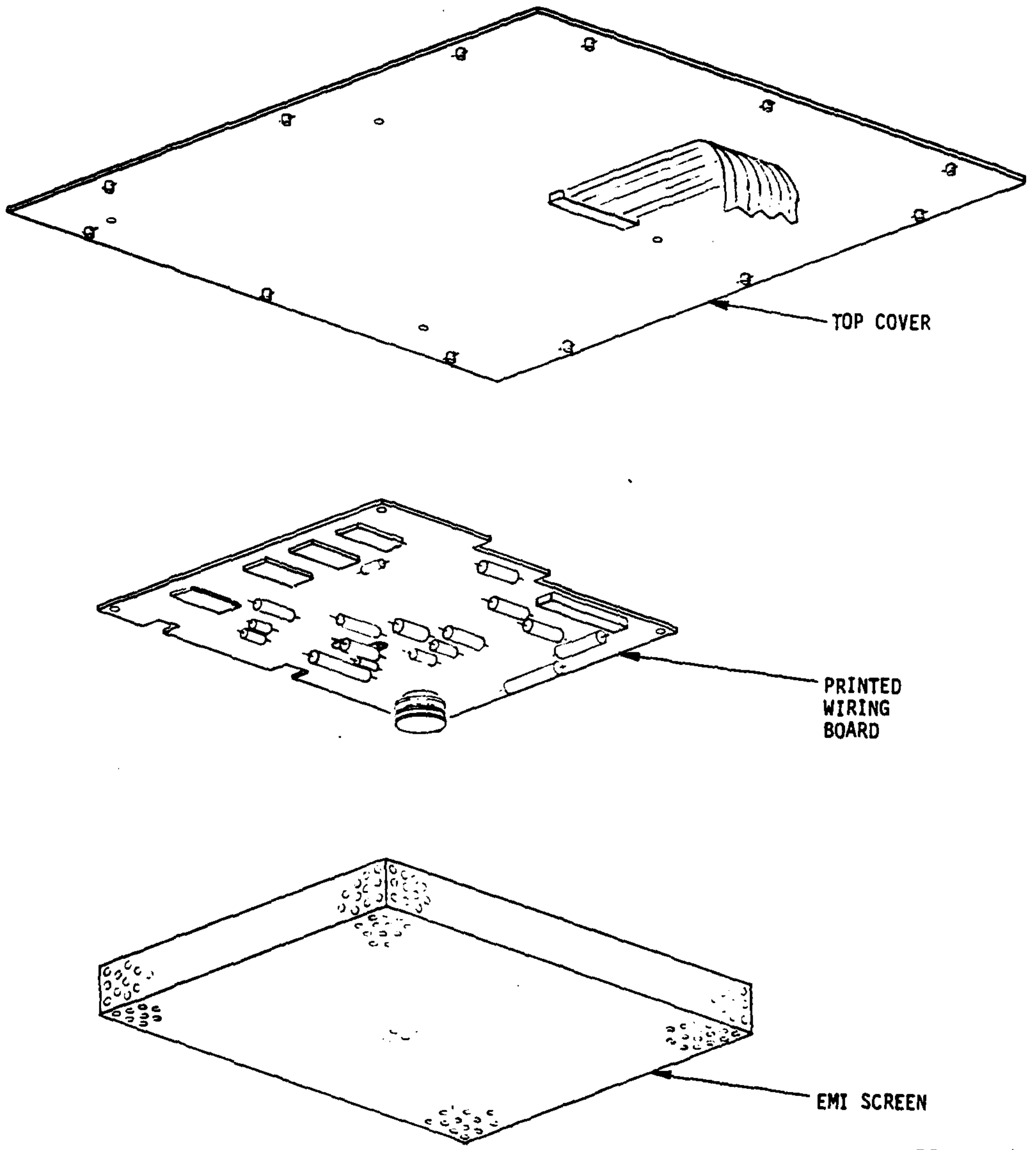


Figure 1-10. Video Amplifier

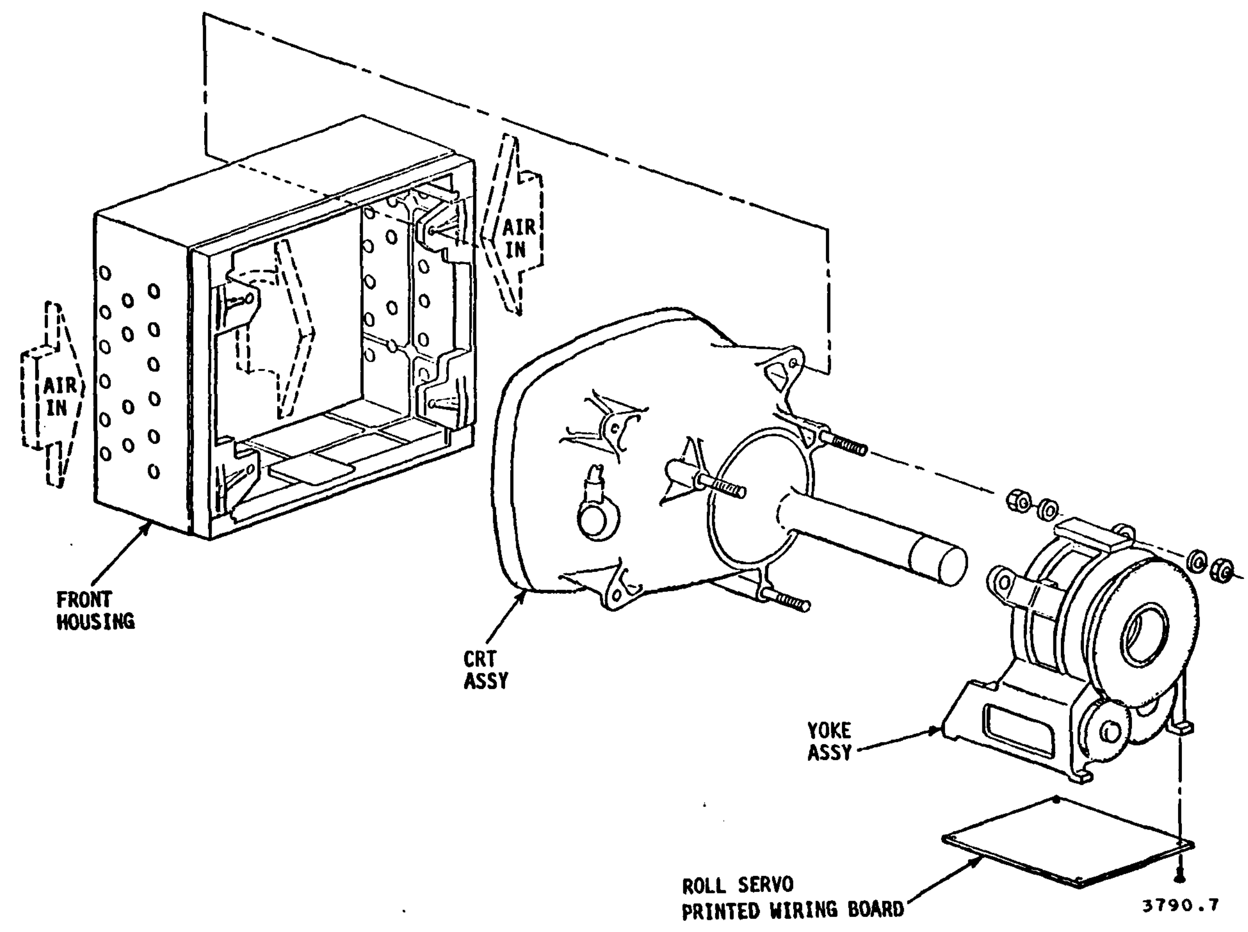


Figure 1-11. Front Housing, CRT & Yoke Assembly

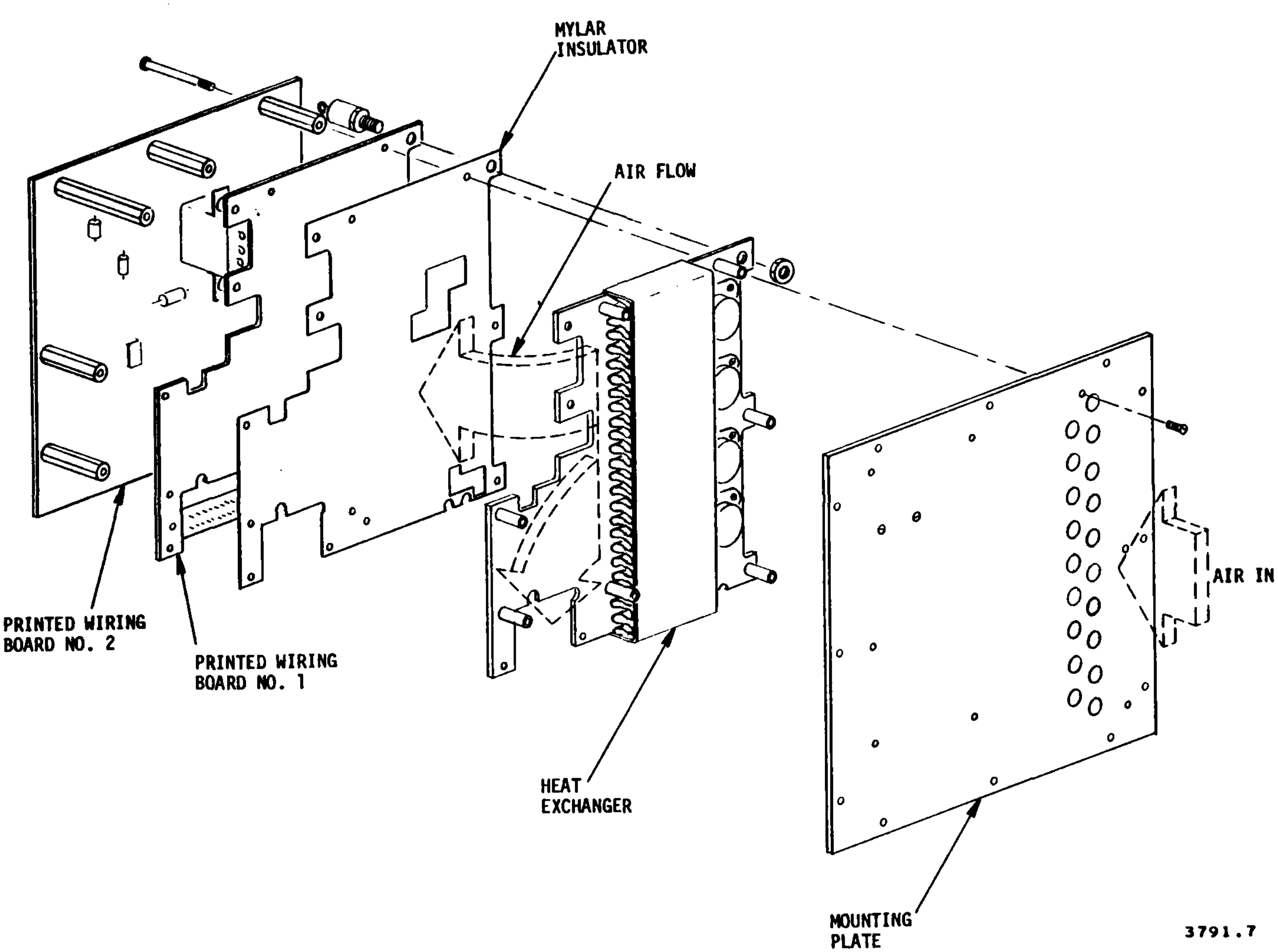


Figure 1-12. Line Scan Deflection Amplifier

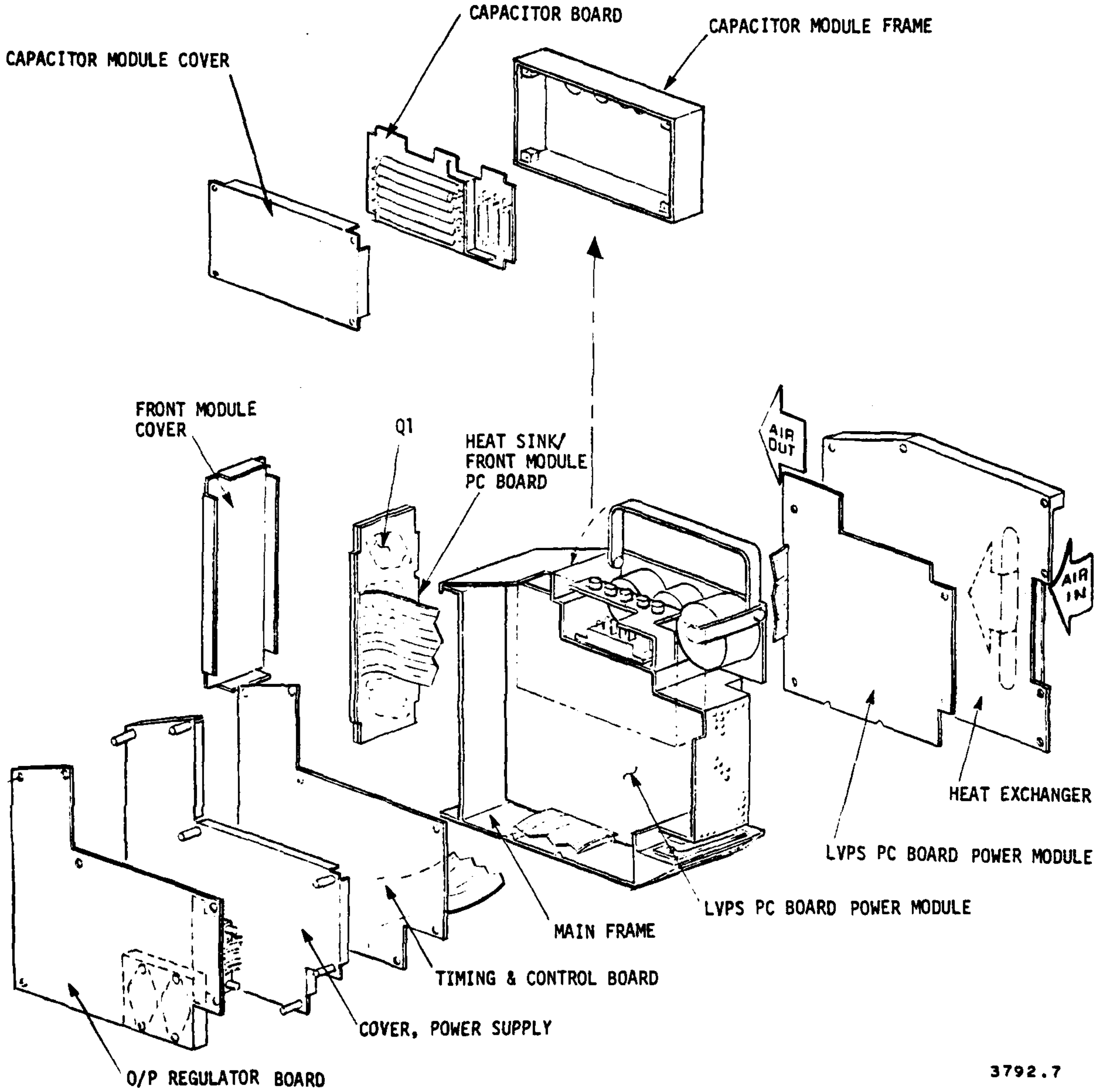


Figure 1-13. Low Voltage Power Supply

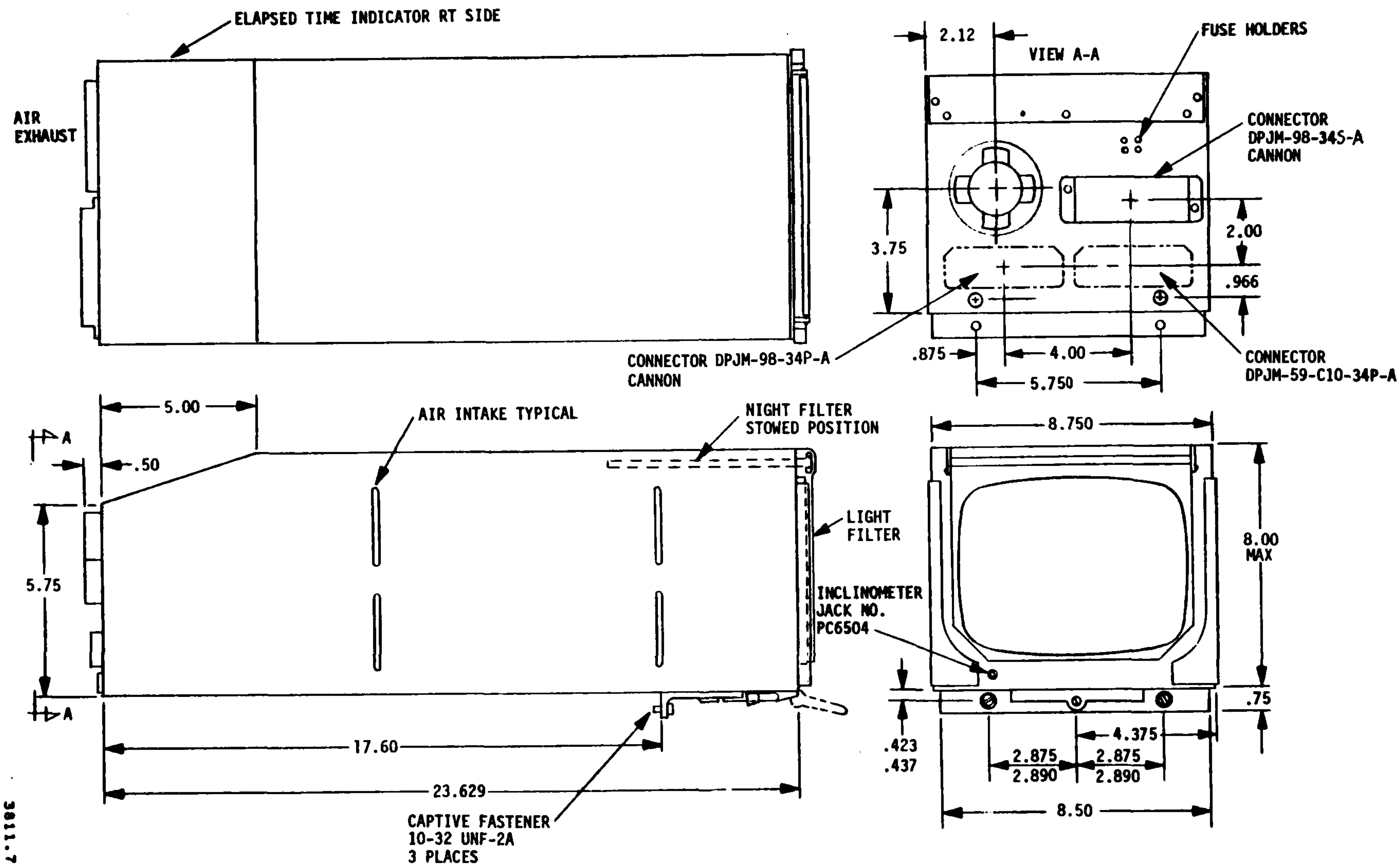


Figure 1-14. Outline Dimensions

1.5.2 Functional Description

The XJ-1 may be functionally divided into two units: a symbol generator and an indicator.

The symbol generator comprises printed circuit boards 1 through 8 and is organized as shown in figure 1-15. Inputs to the symbol generator are the analog inputs from sensors in the various aircraft systems such as the heading synchro, BAGS, radar altimeter, INS, etc. The symbol generator processes these analog inputs in such a manner as to cause a change in its internally generated video signals. These changes may appear on the display symbology as a shift in position, size, appearance, or numeric value.

The indicator comprises a line scan (horizontal) deflection, field sweep (vertical) deflection, video amplifier, roll servo, HVPS, LVPS, and CRT/yoke, and is organized as shown in figure 1-16. The indicator provides a graphic display of the video signals supplied by the symbol generator. These video signals appear on the indicator CRT as numerics, patterns, lines, symbols, etc., giving the pilot essential navigation and tactical information without the necessity of constantly scanning a multitude of panel instruments.

Typical examples are heading, pitch, and radar altitude. The heading symbol on the display is a numeric tape which moves in response to changes in the output from the aircraft heading synchro. The pitch symbol is a group of parallel lines which move up and down to show the pitch attitude of the aircraft in relation to the horizon. The radar altitude symbol is a thermometer-type display consisting of a white line which extends upward from a baseline in response to the output of the radar altimeter.

Returning to figure 1-15, the pitch, pitch trim reference, impact point, VSI, offset impact point, target AOA, CHL, weapon, and radar altitude analog inputs are buffered on board 1, then sequentially selected and converted, one at a time, to 10-bit binary and placed on the data base.

Board 4 picks command heading (steering) data off the data bus, and generates video which represents the heading commanded by the INS. Also, magnetic/true heading data is obtained from the synchro system in the aircraft and synchro data is converted to digital data via hybridized circuitry.

Board 3 picks digitized heading data off the data bus and generates video which appears on the display as a moving numeric tape indicating actual magnetic heading. In addition, board 3 picks off radar altitude data and processes the data to control the vertical length of the radar altitude ribbon. The vertical speed indicator is also generated on this board.

Similarly, board 5 picks off the impact point data and uses it to address a 32 x 16 ROM which generates the impact point symbol.

Board 2 generates the pitch lines, weapon symbol, target symbol, angle of attack error, and offset impact point.

All the above symbols are applied to board 6 where they are selected according to mode inputs received via buffers and symbol control logic, also on board 6, and then mixed into a composite video signal for presentation to the video amplifier in the indicator section.

Board 7 generates the ground texture elements (downward-moving trapezoids), which shift horizontally in response to the phase shift introduced in a 31.5 kHz sinewave by an external azimuth resolver. Board 7 also generates the release marker, which changes position and size in response to inputs from the aircraft computer. The pull-up marker symbology is generated on this board and it changes position and size in response to outputs from the aircraft computer.

Board 8 generates the flight path symbology, which change position, size, and shape in respone to the command altitude, path position, apex position, and radius of curvature inputs from the aircraft computer.

In the indicator, figure 1-16, the video amplifier amplifies the composite video from the symbol generator to an amplitude sufficient to drive the CRT. A gamma correction circuit attenuates the white-level video in a non-linear fashion so as to drive the CRT without saturating it. A sync stripper removes horizontal and vertical sync to operate the line scan and field sweep deflections.

The line scan deflection provides the line-rate sweep current for the CRT yoke. A phase-lock loop insures stable operation at the three sweep frequencies required for the different modes:

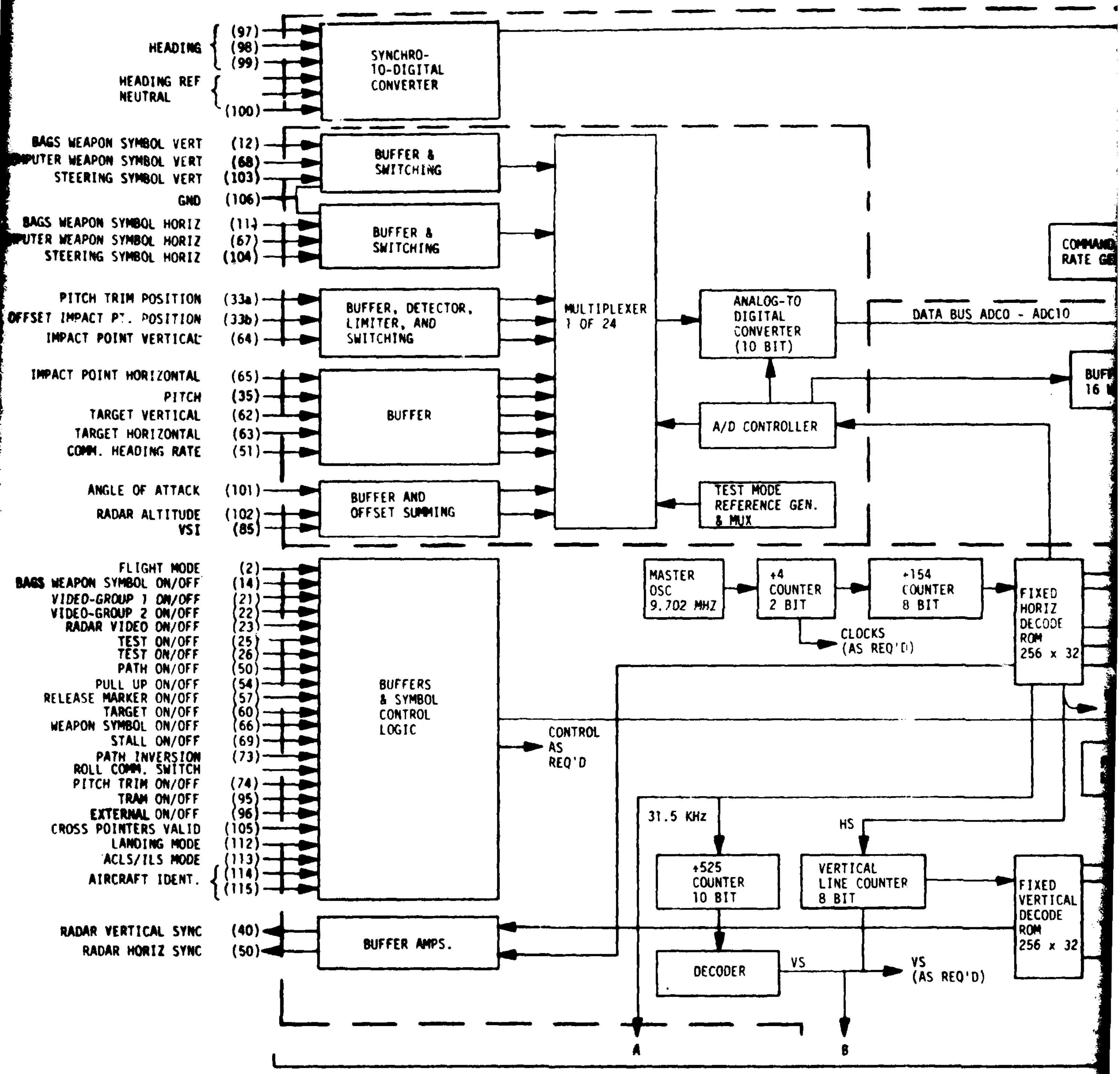
15.75 kHz for ADI and RDC
44.64 kHz for FLIR
15.33 kHz for CONDOR or External Mode

NOTE: External Mode will operate on 15.75 kHz rate

The field sweep deflection provides the 60 Hz field-rate sweep current for the CRT yoke. Sweep characteristics are:

8.33 inch raster, bottom to top for ADI and RDC
7.6 inch raster, left to right for FLIR
5.7 inch raster, top to bottom for CONDOR or External Mode

The roll servo physically rotates the CRT yoke in response to roll commands from the INS, keeping the display earth-stabilized when required by a particular mode.



HEADING
(97)
(98)
(99)
HEADING REF
NEUTRAL
(100)
SYNCHRO-
TO-DIGITAL
CONVERTER
BAGS WEAPON SYMBOL VERT
COMPUTER WEAPON SYMBOL VERT
STEERING SYMBOL VERT
GND
(12)
(68)
(103)
(106)
BUFFER &
SWITCHING
BAGS WEAPON SYMBOL HORIZ
COMPUTER WEAPON SYMBOL HORIZ
STEERING SYMBOL HORIZ
(11)
(67)
(104)
BUFFER &
SWITCHING
PITCH TRIM POSITION
OFFSET IMPACT PT. POSITION
IMPACT POINT VERTICAL
(33a)
(33b)
(64)
BUFFER, DETECTOR,
LIMITER, AND
SWITCHING
IMPACT POINT HORIZONTAL
PITCH
TARGET VERTICAL
TARGET HORIZONTAL
COMM. HEADING RATE
(65)
(35)
(62)
(63)
(51)
BUFFER
ANGLE OF ATTACK
RADAR ALTITUDE
VSI
(101)
(102)
(85)
BUFFER AND
OFFSET SUMMING
MULTIPLEXER
1 OF 24
ANALOG-TO
DIGITAL
CONVERTER
(10 BIT)
DATA BUS ADC0 - ADC10
A/D CONTROLLER
TEST MODE
REFERENCE GEN.
& MUX
FLIGHT MODE
BAGS WEAPON SYMBOL ON/OFF
VIDEO-GROUP 1 ON/OFF
VIDEO-GROUP 2 ON/OFF
RADAR VIDEO ON/OFF
TEST ON/OFF
TEST ON/OFF
PATH ON/OFF
PULL UP ON/OFF
RELEASE MARKER ON/OFF
TARGET ON/OFF
WEAPON SYMBOL ON/OFF
STALL ON/OFF
PATH INVERSION
ROLL COMM. SWITCH
PITCH TRIM ON/OFF
TRAM ON/OFF
EXTERNAL ON/OFF
CROSS POINTERS VALID
LANDING MODE
ACLS/ILS MODE
AIRCRAFT IDENT.
(2)
(14)
(21)
(22)
(23)
(25)
(26)
(50)
(54)
(57)
(60)
(66)
(69)
(73)
(74)
(95)
(96)
(105)
(112)
(113)
(114)
(115)
BUFFERS
& SYMBOL
CONTROL
LOGIC
CONTROL
AS
REQ'D
MASTER
OSC
9.702 MHZ
÷4
COUNTER
2 BIT
÷154
COUNTER
8 BIT
CLOCKS
(AS REQ'D)
FIXED
HORIZ
DECODE
ROM
256 x 32
31.5 KHz
HS
÷525
COUNTER
10 BIT
VERTICAL
LINE COUNTER
8 BIT
FIXED
VERTICAL
DECODE
ROM
256 x 32
RADAR VERTICAL SYNC
RADAR HORIZ SYNC
(40)
(50)
BUFFER AMPS.
DECODER
VS
VS
(AS REQ'D)
A
B

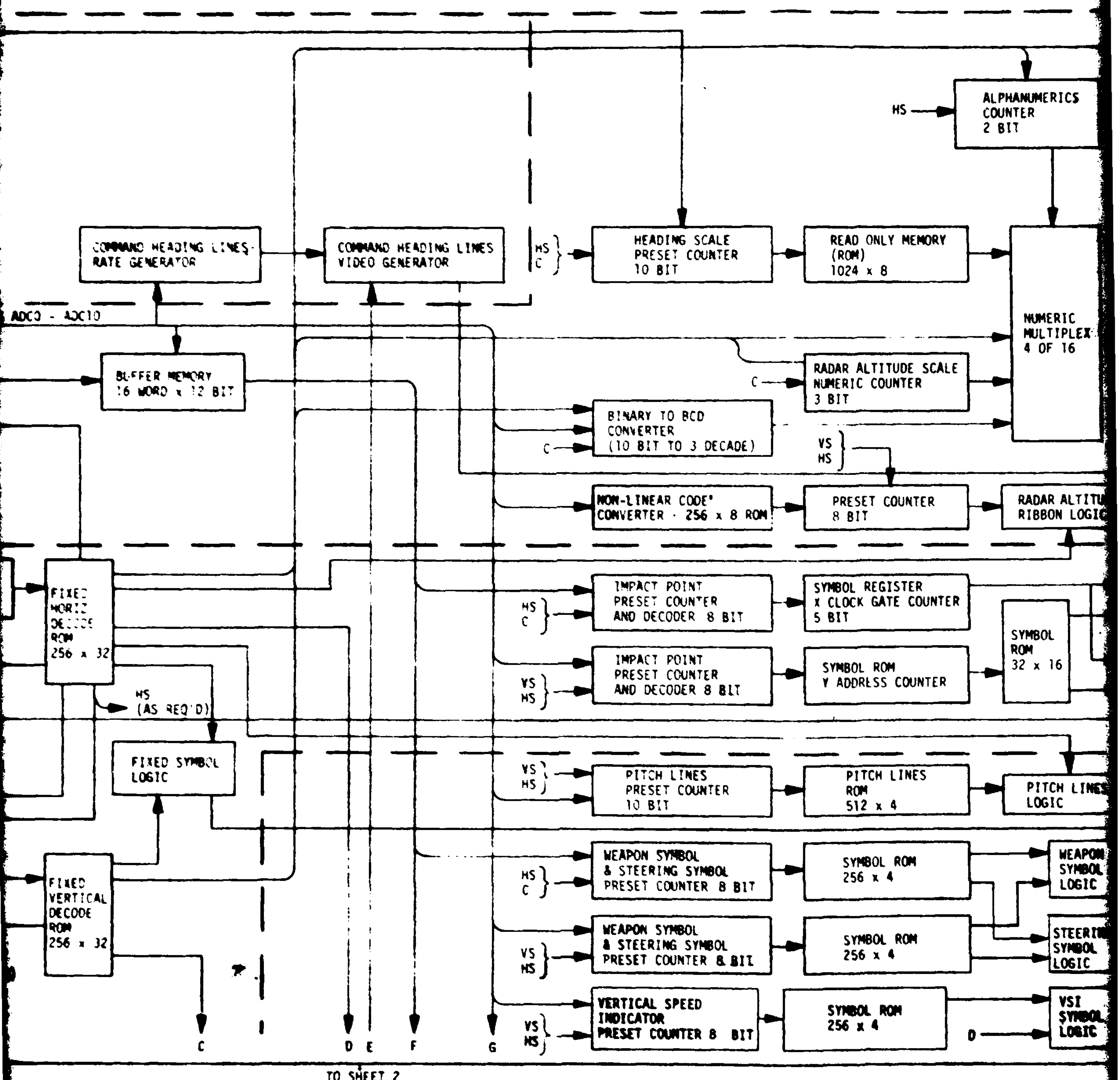
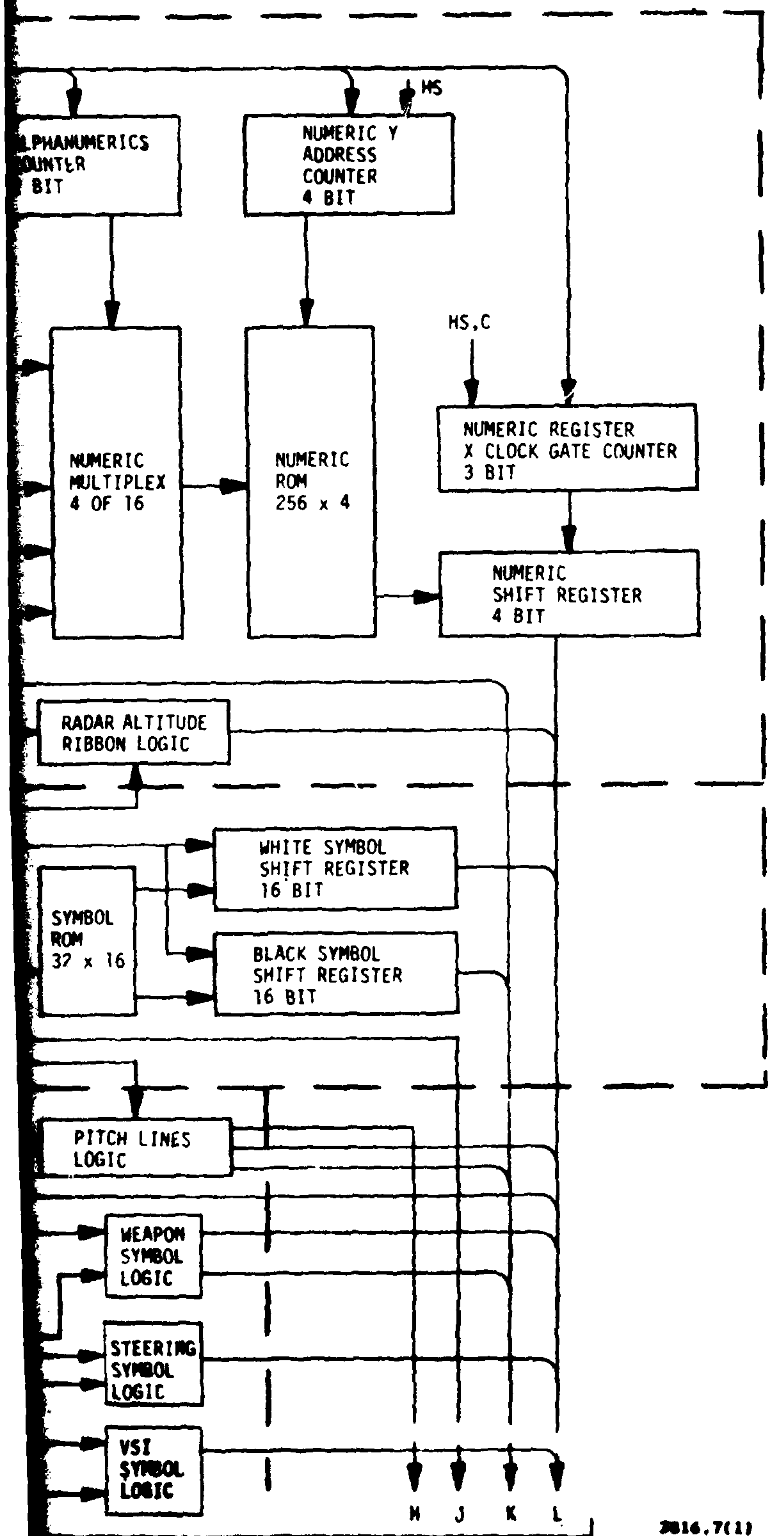


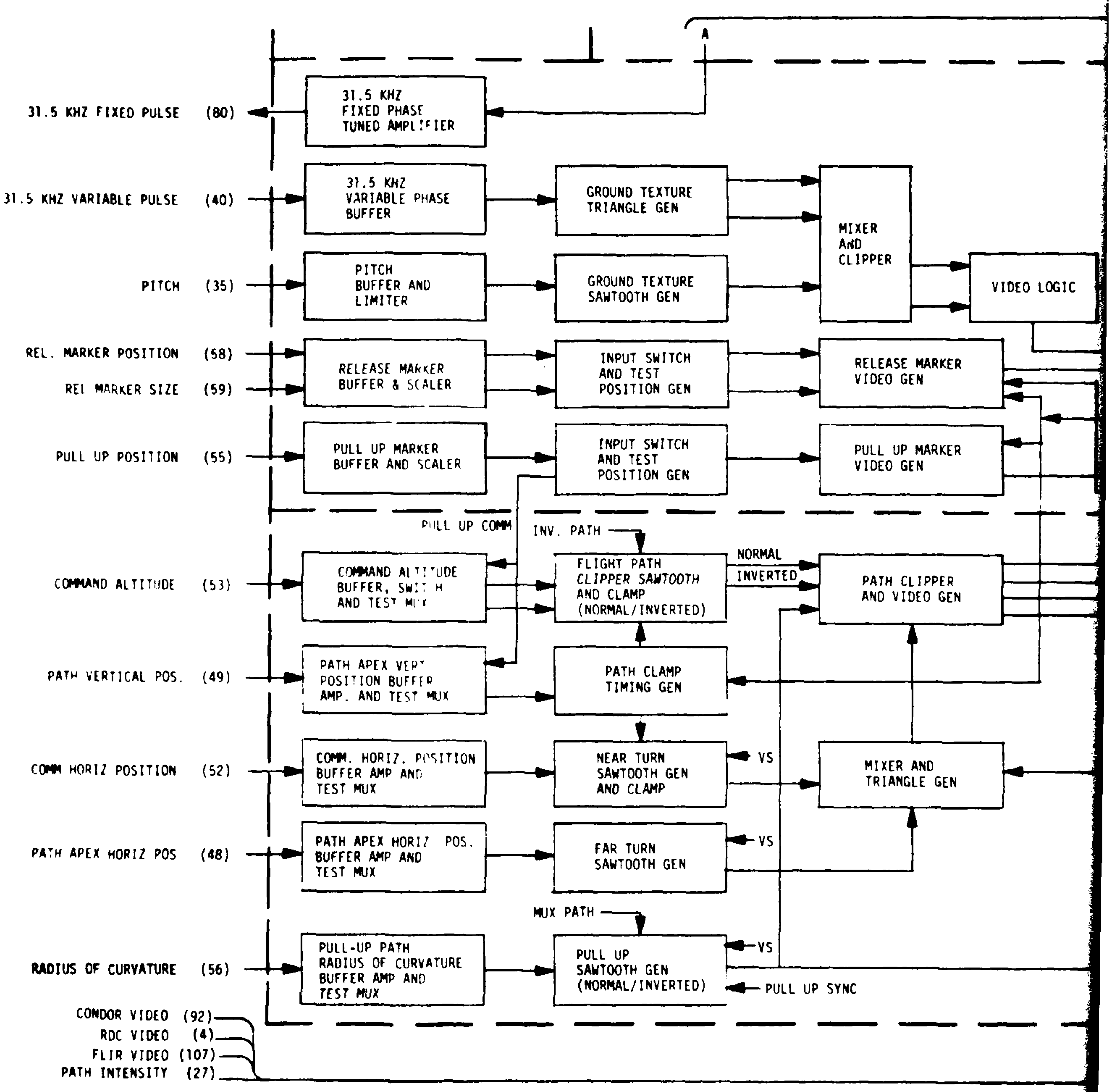
Figure 1-15. Block (

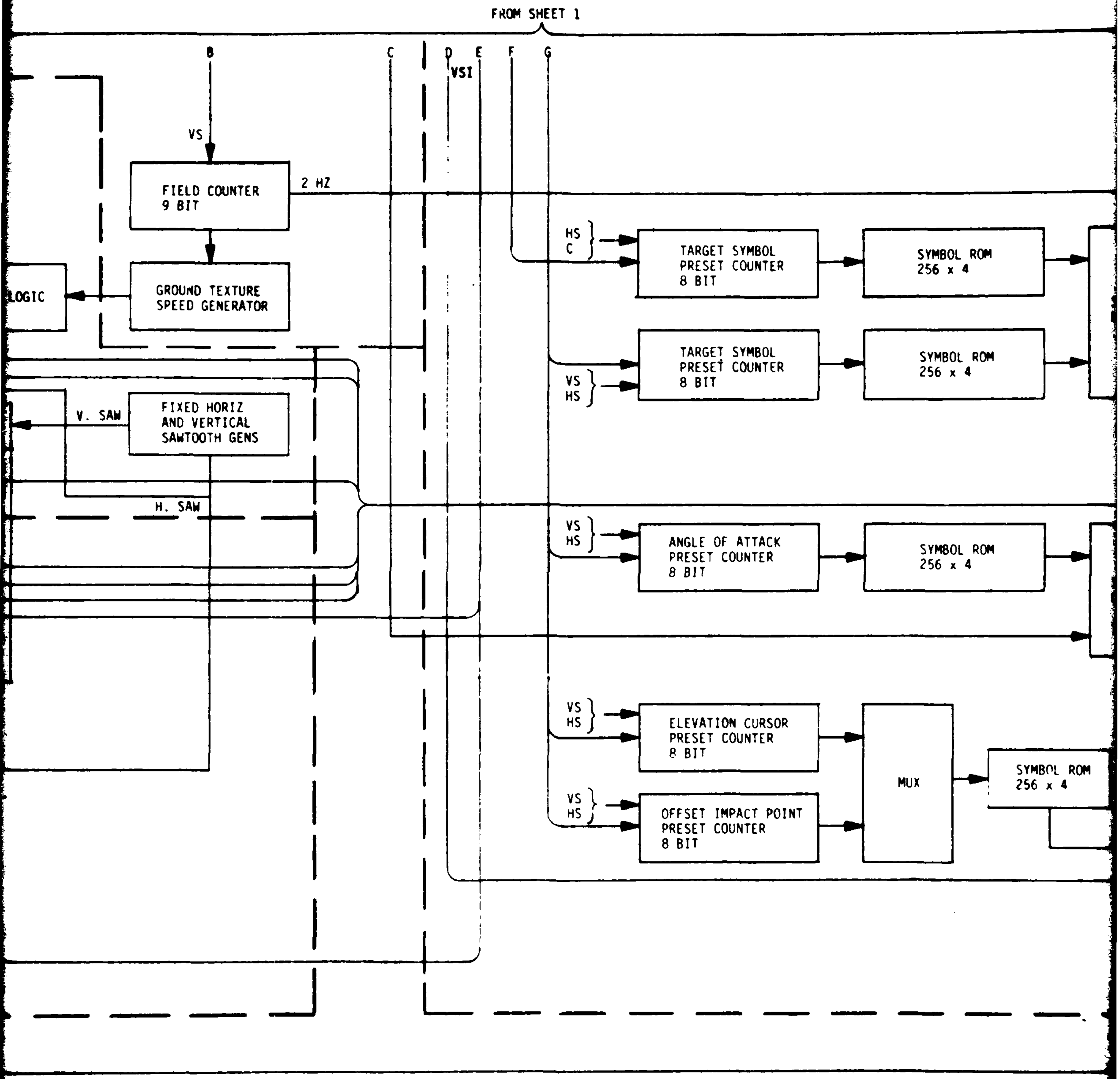
2



Block Generator, Symbol Generator (Sheet 1 of 2)

3


31.5 KHZ FIXED PULSE (80)
31.5 KHZ VARIABLE PULSE (40)
PITCH (35)
REL. MARKER POSITION (58)
REL MARKER SIZE (59)
PULL UP POSITION (55)
COMMAND ALTITUDE (53)
PATH VERTICAL POS. (49)
COMM HORIZ POSITION (52)
PATH APEX HORIZ POS (48)
RADIUS OF CURVATURE (56)
CONDOR VIDEO (92)
RDC VIDEO (4)
FLIR VIDEO (107)
PATH INTENSITY (27)
A
31.5 KHZ FIXED PHASE TUNED AMPLIFIER
31.5 KHZ VARIABLE PHASE BUFFER
GROUND TEXTURE TRIANGLE GEN
MIXER AND CLIPPER
PITCH BUFFER AND LIMITER
GROUND TEXTURE SAWTOOTH GEN
VIDEO LOGIC
RELEASE MARKER BUFFER & SCALER
INPUT SWITCH AND TEST POSITION GEN
RELEASE MARKER VIDEO GEN
PULL UP MARKER BUFFER AND SCALER
INPUT SWITCH AND TEST POSITION GEN
PULL UP MARKER VIDEO GEN
PULL UP COMM
INV. PATH
COMMAND ALTITUDE BUFFER, SWITCH AND TEST MUX
FLIGHT PATH CLIPPER SAWTOOTH AND CLAMP (NORMAL/INVERTED)
NORMAL
INVERTED
PATH CLIPPER AND VIDEO GEN
PATH APEX VERT POSITION BUFFER AMP. AND TEST MUX
PATH CLAMP TIMING GEN
COMM. HORIZ. POSITION BUFFER AMP AND TEST MUX
NEAR TURN SAWTOOTH GEN AND CLAMP
VS
MIXER AND TRIANGLE GEN
PATH APEX HORIZ POS. BUFFER AMP AND TEST MUX
FAR TURN SAWTOOTH GEN
VS
MUX PATH
PULL-UP PATH RADIUS OF CURVATURE BUFFER AMP AND TEST MUX
PULL UP SAWTOOTH GEN (NORMAL/INVERTED)
VS
PULL UP SYNC


FROM SHEET 1
B
C
D
E
F
G
VSI
VS
FIELD COUNTER 9 BIT
2 HZ
GROUND TEXTURE SPEED GENERATOR
LOGIC
FIXED HORIZ AND VERTICAL SAWTOOTH GENS
V. SAW
H. SAW
HS
C
TARGET SYMBOL PRESET COUNTER 8 BIT
SYMBOL ROM 256 x 4
VS
HS
TARGET SYMBOL PRESET COUNTER 8 BIT
SYMBOL ROM 256 x 4
VS
HS
ANGLE OF ATTACK PRESET COUNTER 8 BIT
SYMBOL ROM 256 x 4
VS
HS
ELEVATION CURSOR PRESET COUNTER 8 BIT
VS
HS
OFFSET IMPACT POINT PRESET COUNTER 8 BIT
MUX
SYMBOL ROM 256 x 4

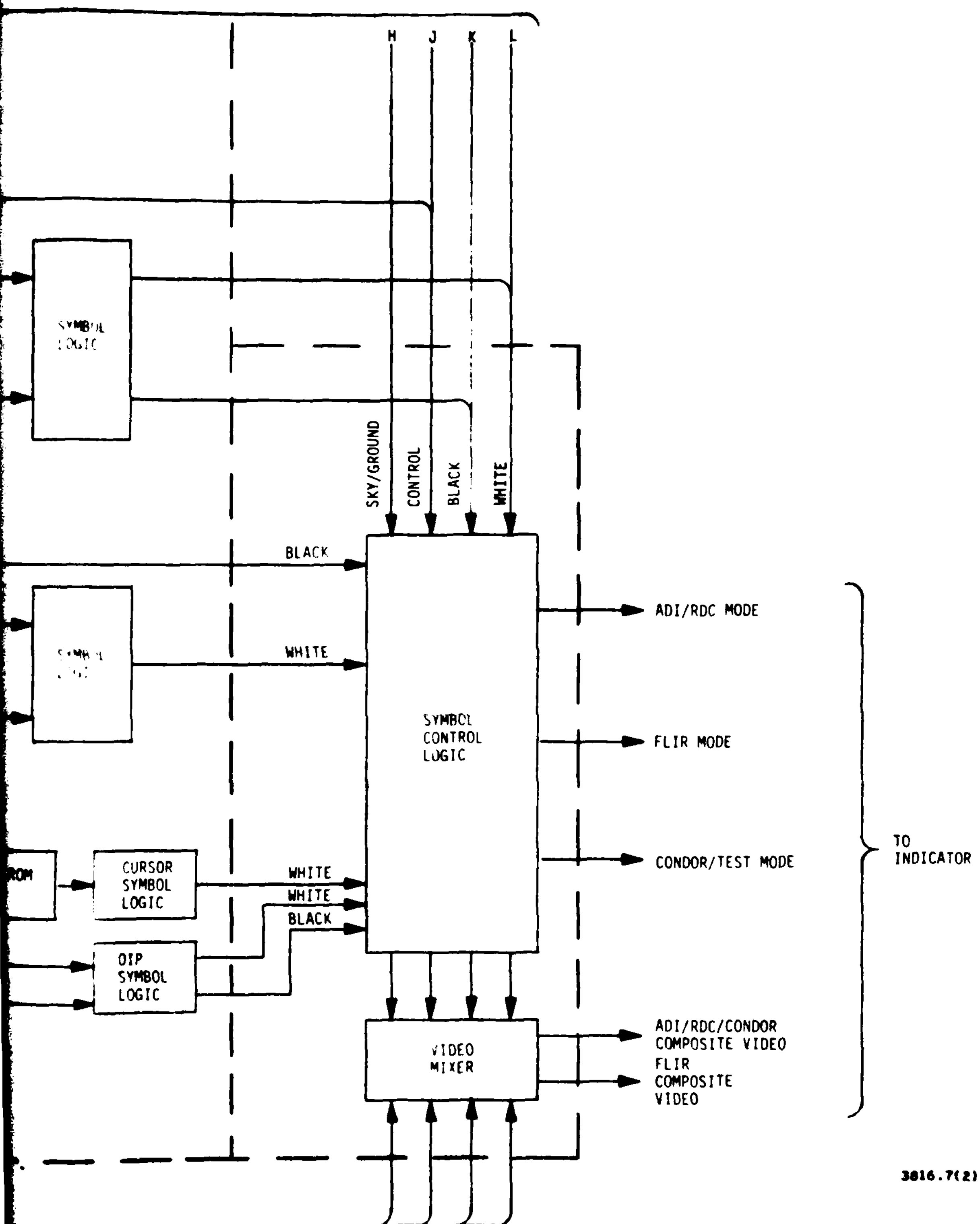
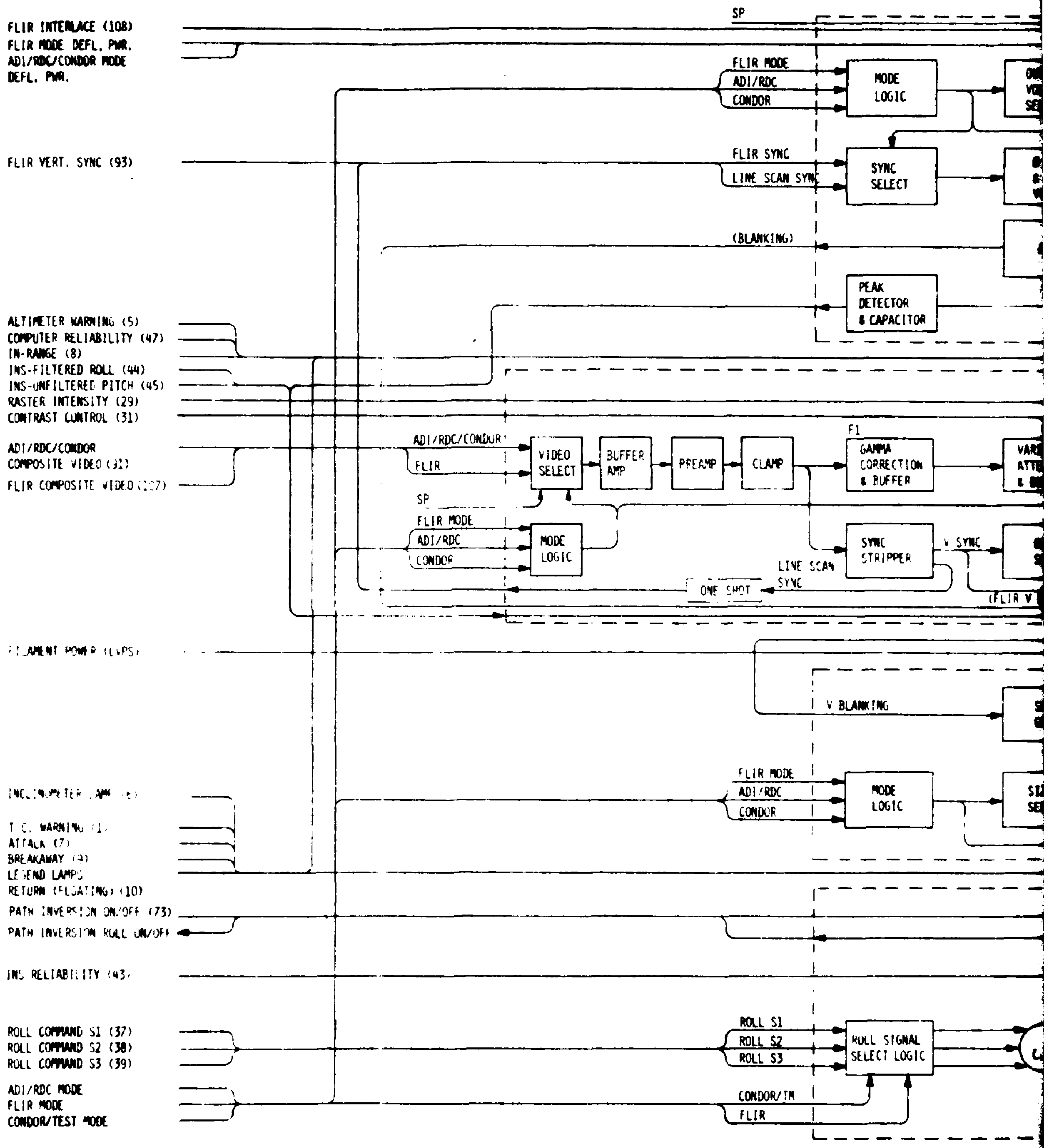


Figure 1-15. Block Generator, Symbol Generator (Sheet 2 of 2)

3


FLIR INTERLACE (108)
FLIR MODE DEFL. PWR.
ADI/RDC/CONDOR MODE
DEFL. PWR.
FLIR VERT. SYNC (93)
ALTIMETER WARNING (5)
COMPUTER RELIABILITY (47)
IN-RANGE (8)
INS-FILTERED ROLL (44)
INS-UNFILTERED PITCH (45)
RASTER INTENSITY (29)
CONTRAST CONTROL (31)
ADI/RDC/CONDOR
COMPOSITE VIDEO (32)
FLIR COMPOSITE VIDEO
FILAMENT POWER (LVPS)
INCLINOMETER LAMP
T.C. WARNING
ATTACK (7)
BREAKAWAY (9)
LEGEND LAMPS
RETURN (FLOATING) (10)
PATH INVERSION ON/OFF (73)
PATH INVERSION ROLL ON/OFF
INS RELIABILITY (43)
ROLL COMMAND S1 (37)
ROLL COMMAND S2 (38)
ROLL COMMAND S3 (39)
ADI/RDC MODE
FLIR MODE
CONDOR/TEST MODE
SP
FLIR MODE
ADI/RDC
CONDOR
MODE LOGIC
FLIR SYNC
LINE SCAN SYNC
SYNC SELECT
(BLANKING)
PEAK DETECTOR & CAPACITOR
ADI/RDC/CONDOR
FLIR
VIDEO SELECT
BUFFER AMP
PREAMP
CLAMP
F1
GAMMA CORRECTION & BUFFER
SYNC STRIPPER
V SYNC
LINE SCAN SYNC
ONE SHOT
V BLANKING
ROLL S1
ROLL S2
ROLL S3
ROLL SIGNAL SELECT LOGIC
CONDOR/TM

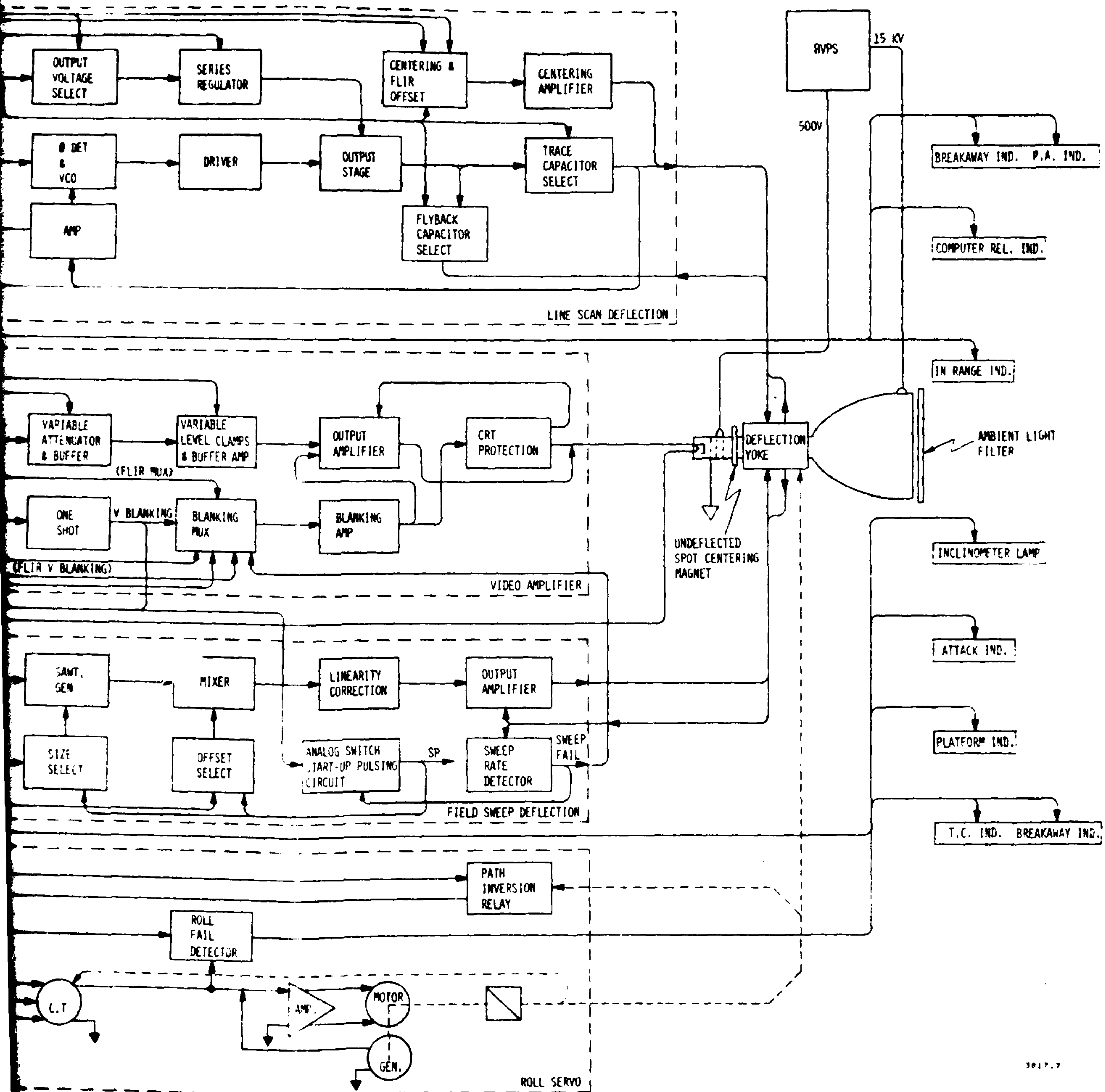


Figure 1-16. Indicator Block Diagram

1.5.3 Modes of Operation

AC and dc voltages are supplied from the aircraft to activate the following modes of operation:

Off
Standby
Contact Analog
Terrain Clearance
Test
TRAM

1.5.3.1 STANDBY MODE. During standby mode of operation, rated voltage is applied to the XJ-1 but not necessarily to the CRT filaments.

1.5.3.2 CONTACT ANALOG MODE. During contact analog mode, the following information is displayed or can be displayed:

(a) <u>Group 1 Video</u>
Impact Point/Stall Symbol
Target Symbol
Weapon Symbol
Pull-up Marker
Release Marker
Path Border and Center Line
Pitch Lines ($+90^{\circ}$, $+60^{\circ}$, $\pm 30^{\circ}$, -40°)
Roll Pointer
Command Heading
True/Magnetic Heading Scale
Angle of Attack Reference and Error Symbol
Altitude Scale
ALS/ILS Steering
VSI Scale and Marker Symbol
ALS or ILS Alphanumerics

(b) <u>Group 2 Video</u>

Horizon

Ground Texture

Pitch Trim Cursor

Pitch Lines (Horizon, $\pm 10^{\circ}$, $\pm 20^{\circ}$)

Flight Path

The pitch trim cursor input (input 33(a)) vertically displaces the pitch trim cursor and the offset impact point marker when the offset impact point marker vertical position input (input 33(b)) is absent. When input 33(b) is present, input 33(a) displaces the pitch trim cursor alone.

1.5.3.3 TERRAIN CLEARANCE MODE. During TC mode, group 1 video information plus the offset impact point marker is displayed or can be displayed. If input 33(b) is present, the pitch trim cursor can also be displayed.

1.5.3.4 TEST MODE. A test switch supplies dc voltages necessary to present test patterns. The patterns consist of all the symbols and markers associated with the contact analog or TC mode, depending on the position of a switch which selects those modes.

1.5.4 Symbol Generator

1.5.4.1 GENERAL. The following paragraphs present detailed descriptions of the printed wiring boards (PWBs) that make-up the symbol generator.

The symbol generator comprises nine printed PWBs as shown in figure 1-9 and listed below.

PWB	ASSY DES.	FUNCTION
1	A4	Analog Input Buffers, A/D Conversion
2	A9	Moveable Symbol Generator
3	A8	Alphanumerics
4	A7	Command Heading, S/O Conversion
5	A10	Timer, Fixed Decode Generation
6	A11	Video Mixer
7	A6	Analog Symbols
8	A5	Flight Path
9	-	Reserved for Growth

Table 1-4 shows the functional partitioning and indicates which of three methods of symbol generation is used for each symbol (analog A, digital D, or hybrid analog/digital A/D).

Table 1-4. Symbol Generator Partitioning

Symbol	Generated or Processed on Board No.									Method of Generation		
	1	2	3	4	5	6	7	8	9	A	D	A/D
Ground Texture						X	X			X		
Impact Point	X				X						X	
Target	X	X									X	
Pitch/Horizon Lines	X	X			X						X	
Horizon Ref.		X									X	
Release							X			X		
Pull-Up							X			X		
Weapon	X	X									X	
VSI	X		X		X						X	
Flight Path								X		X		
Path Border								X	X	X		
Roll Pointer					X						X	
Pitch Trim Ref. Cursors	X	X									X	
Offset Impact Point	X	X									X	
True/Magnetic Heading Scale			X	X							X	
Heading Reference				X							X	
Angle of Attack Error & Ref.	X	X		X							X	
Radar Altitude	X		X		X						X	
Steering		X									X	
Steering Reference					X						X	
Mode Abbreviation (ALS, ILS)			X								X	
Command Heading Lines	X			X								X
Elevation Cursors		X				X					X	

1.5.4.2 BOARD 1 (SCHEMATIC 32011). Board 1 contains the interface circuitry to select and A/D convert the analog input signals from the aircraft sensors. There functions include:

- Analog input buffers and scalers
- Signal multiplexing
- Test mode multiplexing
- Analog-to-digital conversion
- Test mode reference generation

The above functions are combined such that the analog signal inputs are sequentially multiplexed to an analog-to-digital converter. Upon application of a TEST MODE command, the test mode reference voltages are sequentially multiplexed instead of the input signals.

Figure 1-17 is a block diagram for the board. Analog input data is scaled through resistor dividers or op amps, then routed to three eight-channel analog multiplexers. These multiplexers are sequentially addressed by a counter which is clocked at 31.5 kHz during vertical blanking. This counter drives the analog multiplexers which allow the analog data to be multiplexed to an A/D converter.

The A/D converter has a maximum input range of $\pm$10V, with an input data scale factor of 9.8 mV/bit. The converter output, eleven bits of parallel data $\overline{\text{ADC0}}$ through $\overline{\text{ADC10}}$, is routed to the other boards for further processing.

In test mode another set of multiplexers are addressed. The inputs of these come from a resistor divider network which supplies various dc voltages to simulate the operational inputs.

1.5.4.3 BOARD 2 (SCHEMATIC 32021). Board 2 contains the circuitry to generate the pitch lines, pitch reference cursors, angle-of-attack error, offset impact point, target, weapon, and ALS/ILS steering bars.

Figure 1-18 is a block diagram of the board. The pitch symbols are generated by a vertical position counter and ROM. Data from the A-to-D converter is preset into the vertical counter, which is then clocked by horizontal blanking.

The ROM output is gated with fixed horizontal decode inputs to provide the pitch symbol video. The weapon symbol and steering symbols have a horizontal position counter and a vertical position counter. Data from the A-to-D converter is preset into both counters and these counters address their respective ROM's. The horizontal position counter is clocked by a 4.851 MHz clock. The ROM outputs are fed through combinatorial logic to provide the weapon symbol and steering symbol video.

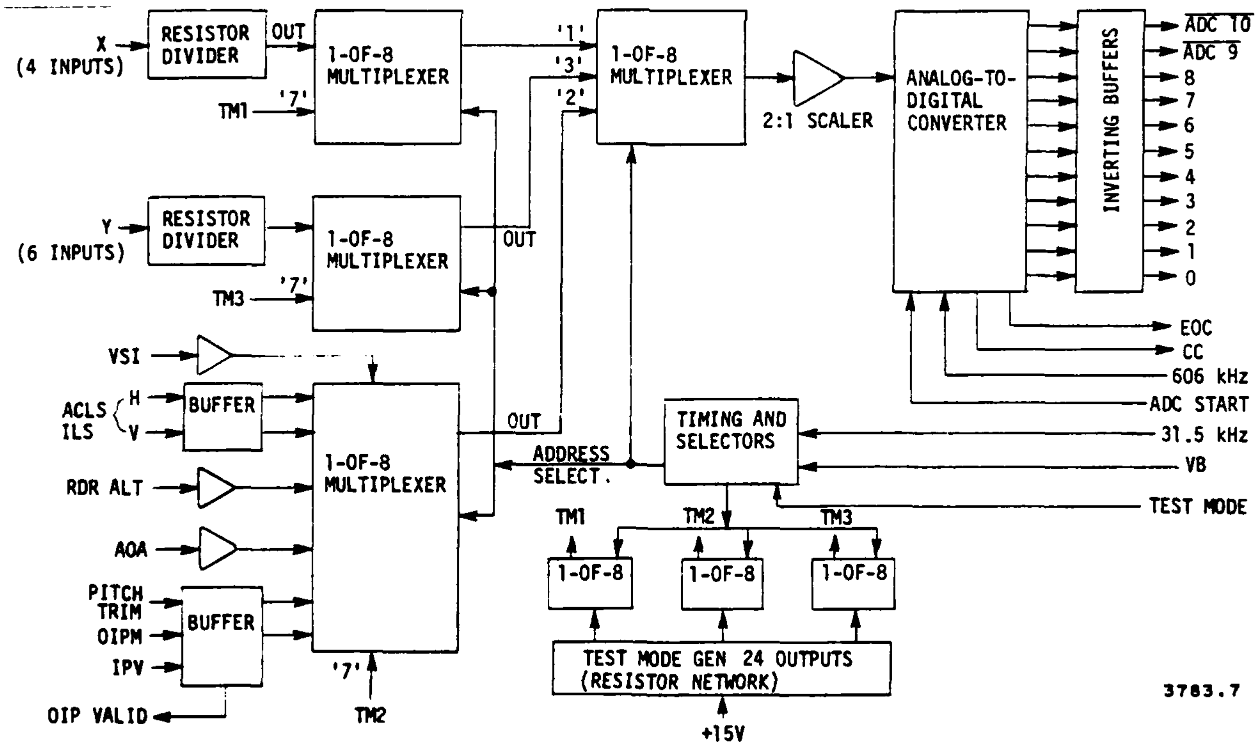


Figure 1-17. Board 1 Block Diagram

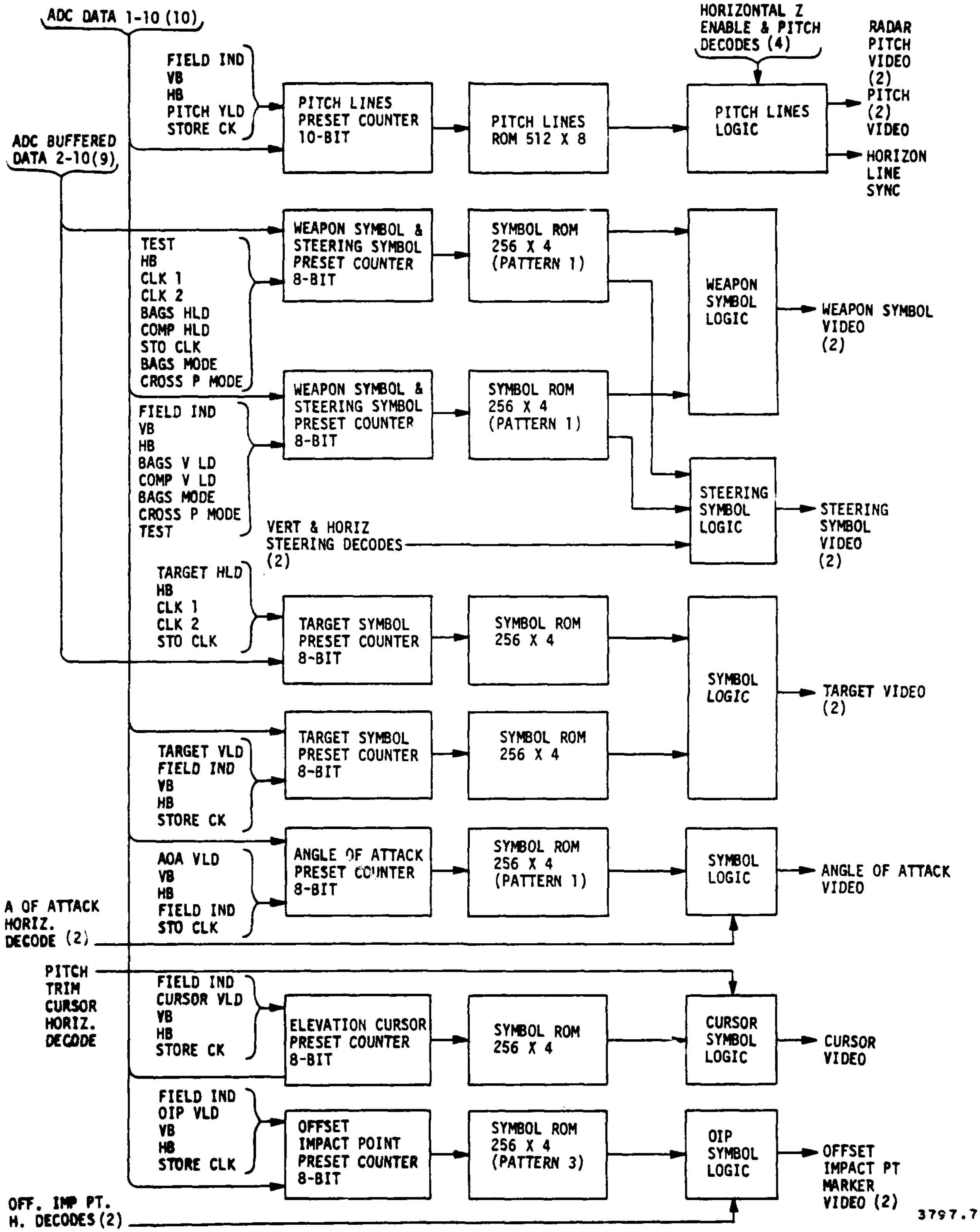


Figure 1-18. Board 2 Block Diagram

The other symbols are generated in a similar manner. The target symbol video is generated from a horizontal position counter and vertical position counter and ROM's.

The angle of attack error has only a vertical position counter. The ROM output is gated with fixed horizontal decode inputs to provide the angle of attack error video.

The pitch trim cursor and offset impact point marker have a vertical position counter. Each is gated with the appropriate horizontal decodes to generate the elevation cursor video and the offset impact point marker video.

The following paragraphs present a detailed discussion of the various operations summarized above.

- Pitch Lines. The pitch lines are slightly more complicated than the other board 2 symbols, requiring data bits 1 through 10. A data bit 1 change moves the pitch lines 1 line/frame. Total pitch range is $+90^{\circ}$ to -90°.

When input data is all 0's, the horizon appears in the center of the screen at ROM address 125, as shown in figure 1-19.

According to specification, the display has 60 degrees of pitch vertically. This means that with the horizon in the center of the screen, part of the $+30^{\circ}$ line and part of the -30° line should be visible.

As a result, the $+30^{\circ}$ line appears centered on ROM address $\left[125 + 125 \left(\frac{5.2"}{8.33"}\right)\right] = 203$ that is $\left[\text{horizon address + addresses from center of display to raster edge} \times \frac{\text{display size}}{\text{raster size}}\right]$.

Outputs from the pitch line circuitry are the various pitch lines, SKY/$\overline{\text{GROUND}}$, and horizon line sync (S HORIZON).

- ROM Disable Flip-Flop. Note on figure 1-19 that addresses 281 through 511 are used for $+60^{\circ}$ and $+90^{\circ}$ pitch lines. For pitch below -40°, no negative pitch lines are displayed. These negative pitch areas wrap around and also address 277 through 511. To prevent the $+60^{\circ}$ and $+90^{\circ}$ pitch lines being displayed when the negative pitch lines were preset, a ROM disable flip-flop is set when ROM OUTPUT-ROM DISABLE occurs, because it was preset to that value. This flip-flop resets when count 512 is reached. When the ROM disable flip-flop is set, SKY/$\overline{\text{GROUND}}$ goes to ground, and $+60^{\circ}$ and $+90^{\circ}$ pitch line outputs are inhibited.

- Horizon Line Sync. HORIZON LINE SYNC is used to start the ground texture generators. As a result, it must always occur, not just when the horizon line is visible. When the horizon is not present an artificial horizon line is produced by the horizon line sync circuitry.

An added complication is that when ADC data bit 1=1 for the pitch lines, HORIZON LINE SYNC still needs to have the same address outputs for both fields. The reason for this is that the vertical decodes of the ground texture will not move smoothly down the screen unless this is done.

To generate HORIZON LINE SYNC, another horizon decode is provided (P1) one address off from horizon. When the horizon is moved down one bit because of ADC data bit 1=1, the horizon line sync circuitry picks the other decode during even fields and moves HORIZON LINE SYNC up one bit from horizon.

- Other Movable Symbols. All symbols on this board are set up with a data structure similar to the pitch line. Symbol counters are preset with a load pulse and a clock associated with the load, called GEN STORE CLOCK. The counters of the vertically moving symbols are preset during vertical blanking. When the preset is all 0's, the symbol appears in the vertical center of the screen, corresponding to ROM address 125. A positive number moves the symbol downward from zero, a negative number moves it upward; the data is ADC data bit 2 through 10 for symbols other than the pitch lines. Horizontally, counters are preset during horizontal blanking. When all 0's are present the symbol is in the horizontal center of the screen, corresponding to ROM address 125.

The pitch lines, pitch trim cursor, angle of attack, and offset impact point marker move only vertically, and the horizontal portion of each is generated from fixed horizontal decodes.

- Programming of Pitch Line ROMs. Figure 1-19 shows the position of the various decodes within the ROMs, as well as a chart for the actual programming.

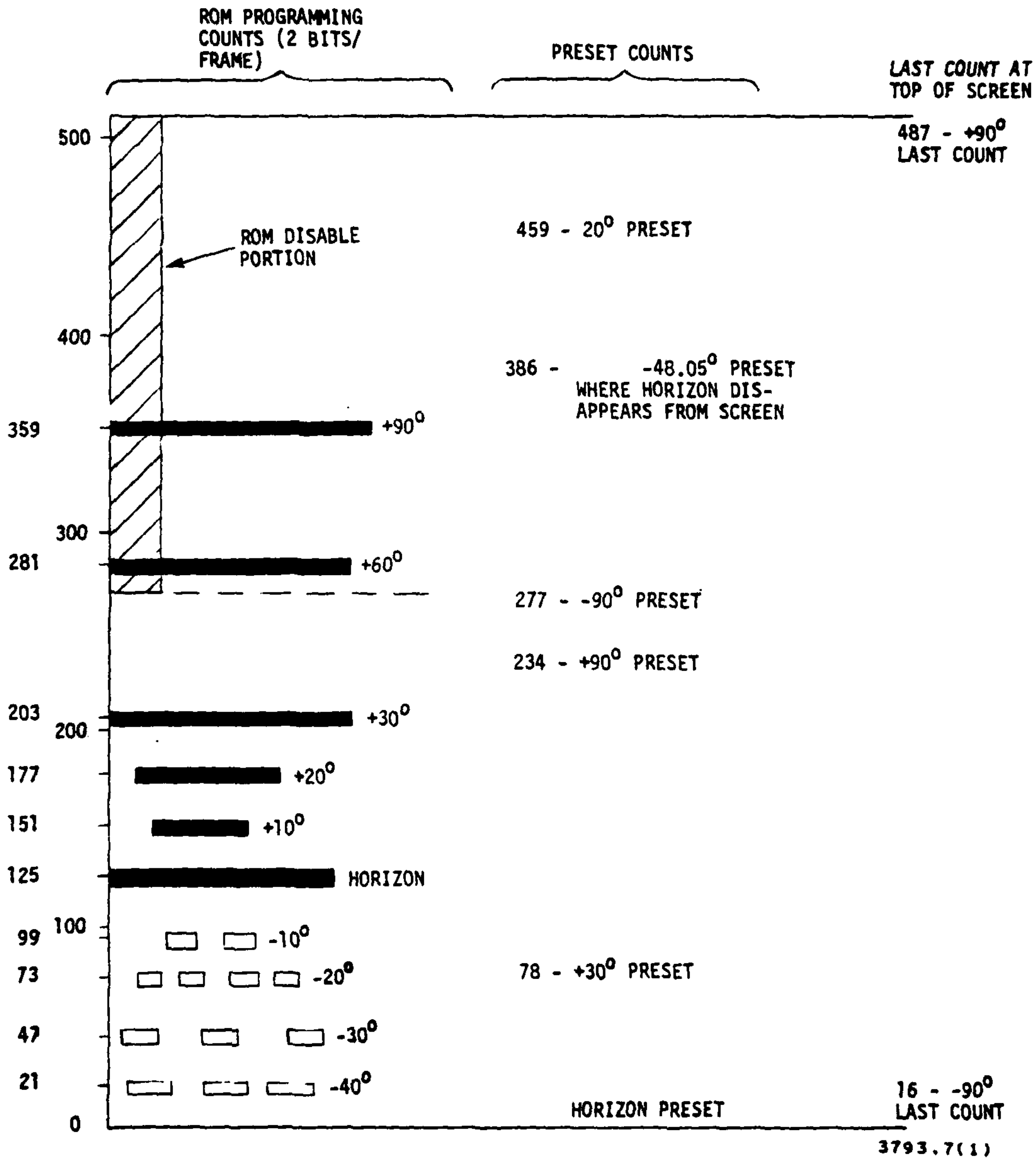


Figure 1-19. Pitch Lines ROM Programming (Sheet 1 of 3)

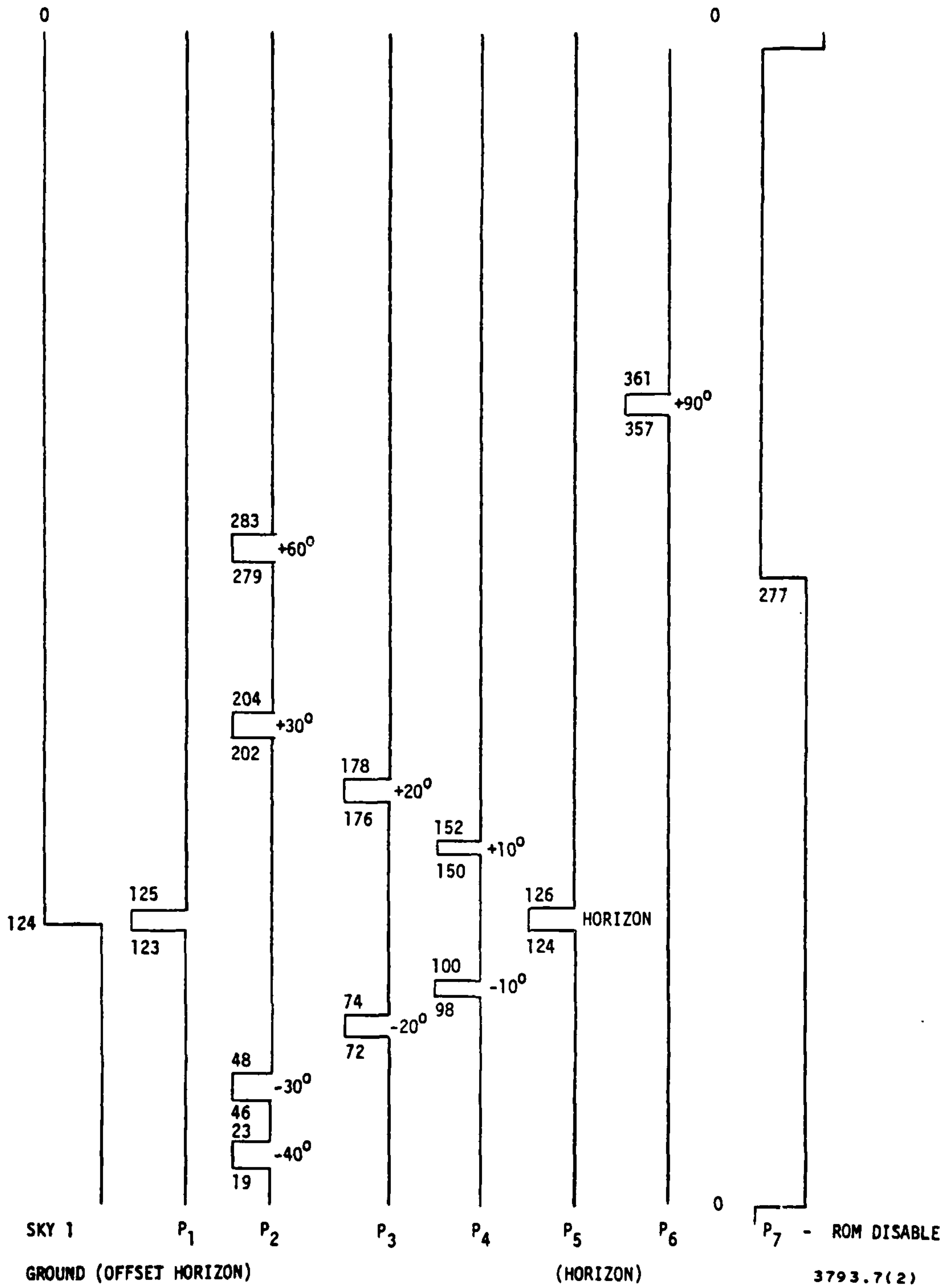


Figure 1-19. Pitch Lines ROM Programming (Sheet 2 of 3)

$96.1^\circ = 250$ BITS/FIELD

	INPUT	$\frac{\text{INPUT}}{2}$	ROM PROGRAMMING: (CENTER COUNT OF LINE) ADD OFFSET OF 125	LAST COUNT AT TOP OF SCREEN
-96.1°	-500	-250	-125 → 386	0
-90°	-468	-234 → 277	-109 → 402	16
-48.05°	-250	-125 → 386	0	125
-40°	-208	-104 → 407	21	146
-30°	-156	-78 → 433	47	172
-20°	-104	-52 → 459	73	198
-10°	-52	-26 → 485	99	224
0°	0	0	125	250
$+10^\circ$	52	26	151	276
$+20^\circ$	104	52	177	302
$+30^\circ$	156	78	203	328
$+60^\circ$	312	156	281	406
$+90^\circ$	468	234	359	484

Figure 1-19. Pitch Lines - ROM Programming
(Sheet 3 of 3)

Two ROMs cover addresses 0 through 225. Two additional ROMs cover addresses 256 through 511; the actual addresses are the numbers on the chart, minus 256.

• Programming of Other Symbol ROMs. The ROMs for symbols other than the pitch lines are relatively simple. Symbol sizes were determined from the specification at 1/30" per ROM address with symbols centered around ROM address 125.

Two pattern 1 ROMs are used for the steering bars and weapon symbol. The 0_4 output is u ed for the steering bars, the 0_3, 0_2 and 0_1 outputs for the weapon symbol. Output 0_1 defines the inside of the weapon symbol, 0_2 the white portion, and 0_3 the block portion.

The target symbol, pitch trim cursor and offset impact point marker use pattern 3 ROMs, however, different outputs are used to generate the various symbols.

The target symbol, weapon symbol, and ALS/ILS steering bars move vertically and horizontally. The weapon symbol and ALS/ILS steering bars are generated using the same counters and ROMs, but by multiplexing the load pulses and ROM outputs. A mode line from board 6, CROSS PNTRS/$\overline{\text{WEAPON}}$, selects the symbol to be displayed. When the display is in the cross pointer mode, a reference square is displayed, which turns black when the ALS/ILS steering bars overlay it.

1.5.4.4 BOARD 3 (SCHEMATIC 32031). Board 3 provides the following primary functions:

- Stores 16 symbol position points from the ADC in a digital buffer memory.

- Translates and decodes the magnetic heading SDC data into a two-digit numeric code, and 5^{o} and 10^{o} index marks.

- Provides a single breakpoint two-scale-factor code converter for the altitude signal, and generates 0-thru 2-digit altitude scale numerics

- Provides the code generator for the ALS/ILS characters

- Generates the altitude thermometer indicator and associated numerics.

- Generates the horizontal and vertical raster components of the four alphanumeric character generators.

- Generates vertical speed indicators

Figure 1-20 illustrates how the above functions are accomplished. Figures 1-21 and 1-22 show vertical and horizontal timing.

Quantized symbol position data from the ADC is stored in the buffer memory. Three 16 x 4 bit RAM's provide 16 words by 12 bits of storage; 11 of the 12 possible bit locations are connected to the ADC. Timing logic permits writing of data into the buffer memory during vertical blanking, and reading of data from the memory during horizontal blanking. Addresses to the buffer memory are decoded by 1-of-24 logic, and are used for the vertical and horizontal load pulses. Data selection is thus accomplished by load pulse timing.

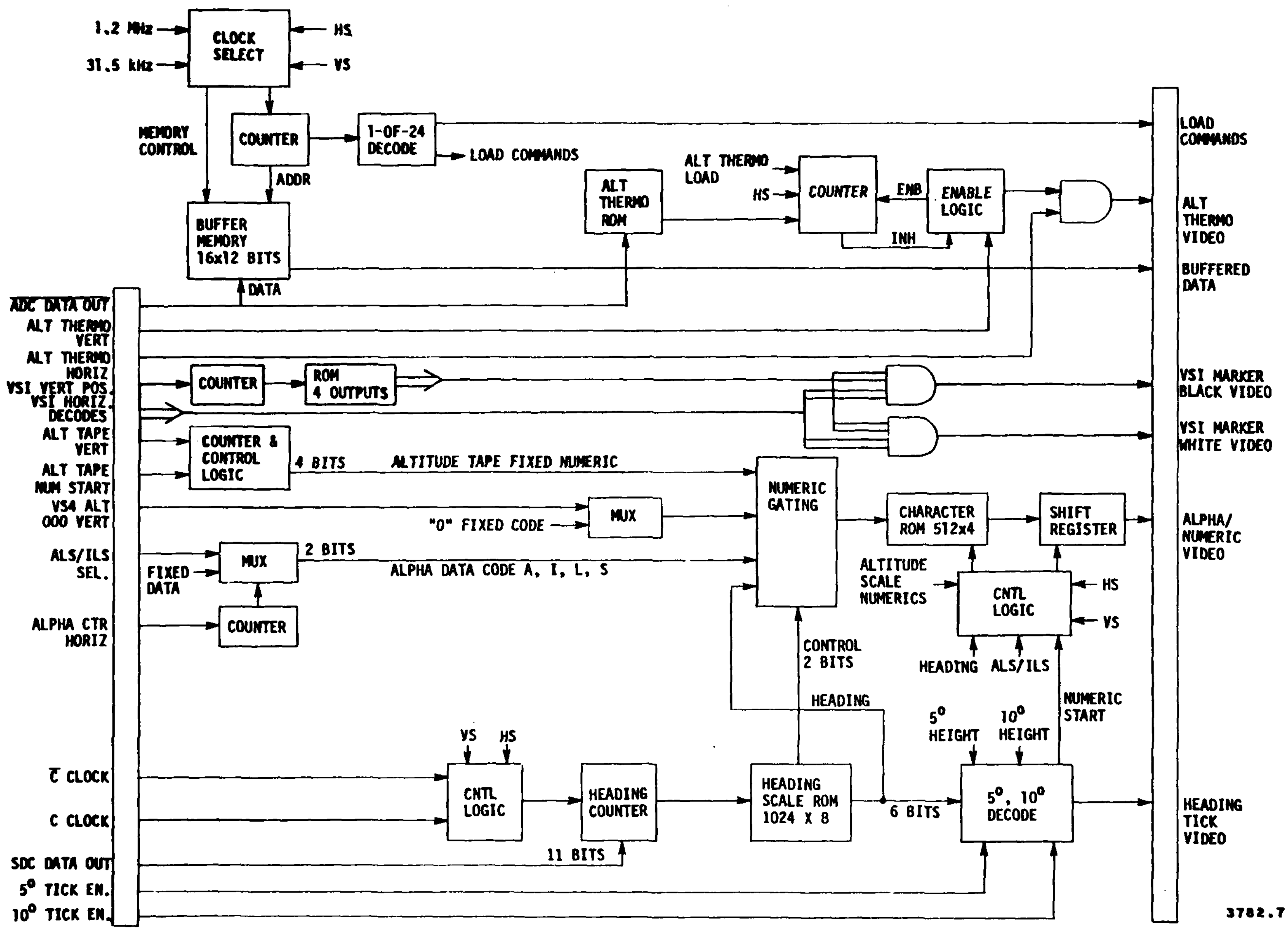


Figure 1-20. Board 3 Block Diagram

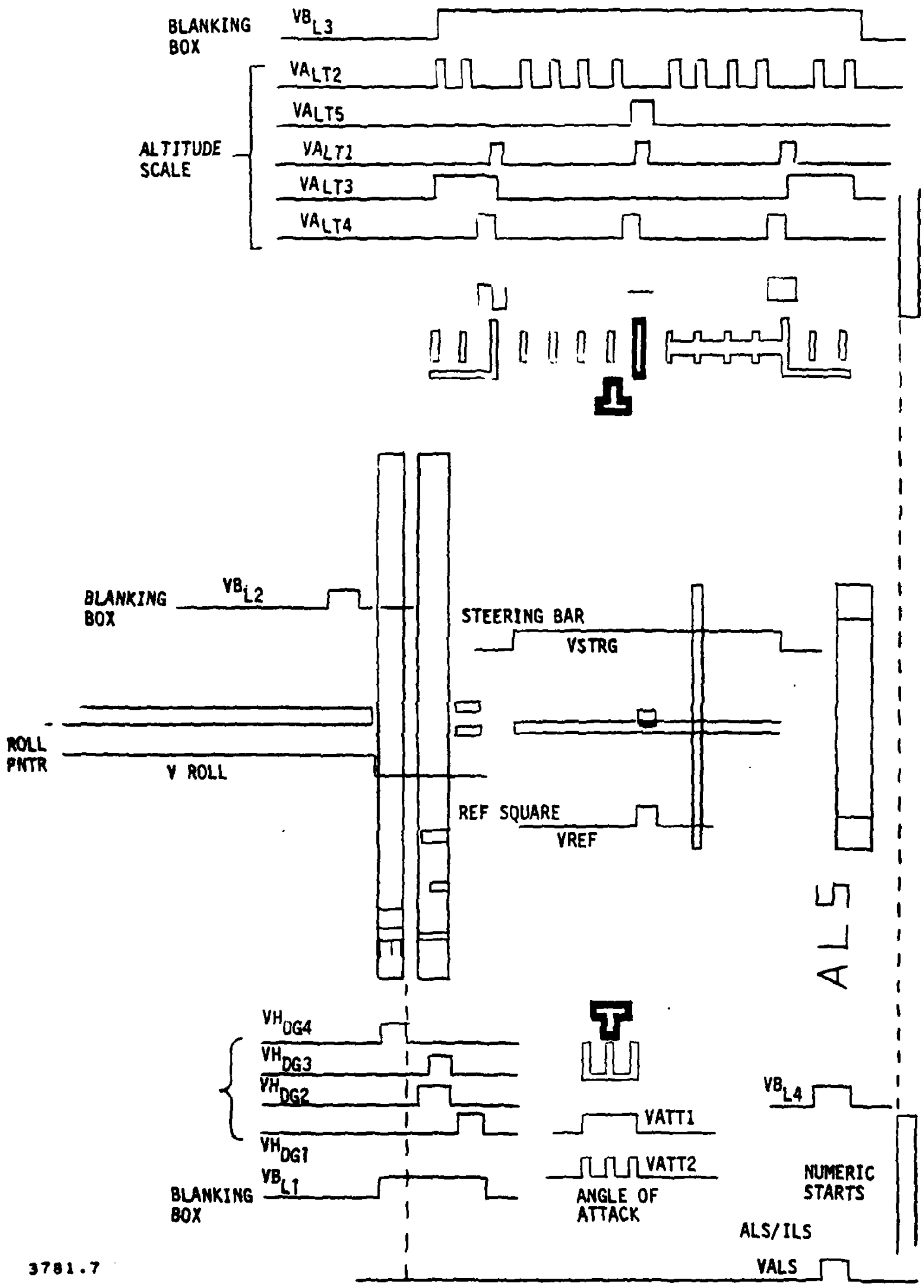


Figure 1-21. Vertical Timing

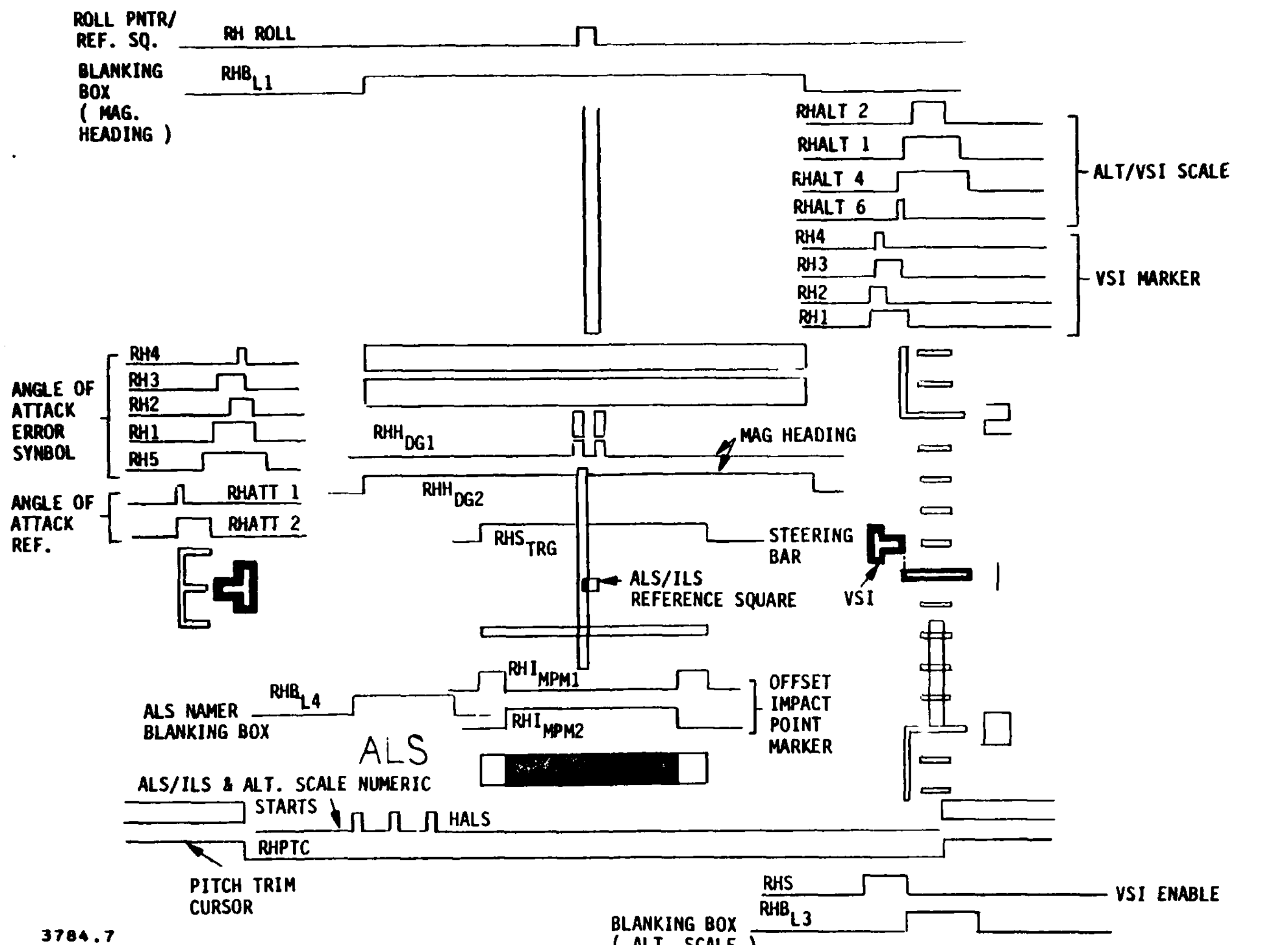


Figure 1-22. Horizontal Timing

Eleven bits of magnetic heading data, from the SDC on board 4, are translated and decoded to provide the heading scale hundreds and tens digits, and the 5^{0} and 10^{0} index marks. SDC data is loaded into an 11-bit binary counter; offsetting of the heading scale, so that the SDC data point coincides with the center of the raster, is accomplished by translating the decoding structure of the heading scale PROM one-half of the horizontal display distance. Organization of the PROM is 1024 words by 8 bits, with 2 bits for the hundreds digit, 4 bits for the tens digit, and 2 bits of steering data to designate either tick marks or digits.

Generation of the numerics is performed by a 10-bit binary to 3-decade BCD converter. Included in the converter are two scale factors, selected as a function of the ADC sign bit (sign bit 0 indicates altitude above 400 ft.). Whenever the sign bit is 1, designating an altitude below 400 feet, a 1:7.5 prescaler is switched into the converter clock circuitry to calculate altitudes below 400 feet.

The altitude thermometer bar circuitry uses an eight-bit binary counter, programmed with the equivalent height of the bar in horizontal scan lines. The counter is started at the beginning of the altitude scale outline, enabling display of the bar, and continues until the 8-bit counter generates a carry out, inhibiting display of the bar.

A four-bit counter and quad-multiplexer encode the alpha characters A, I, L, S. A single input line selects either the ALS or ILS display, decoding the A or I character. The L and S characters are always decoded at their proper raster position.

An alphanumeric ROM, along with vertical and horizontal control logic, generates the alphanumeric characters in the raster pattern. A particular character is selected when the beam scan moves within the symbol blanking box.

The following paragraphs present a detailed discussion of the various operations summarized above.

- Load Counter. The 1-of-24 load counter is clocked at 31.5 kHz during vertical blanking and at 1.2 MHz during horizontal blanking.

During vertical blanking the 1-of-24 load counter counts 24 periods. Each period is decoded by the symbol generator load logic, which generates various load pulses. The first nine load pulses are for horizontal data, during which time the ADC data is written into a buffer storage memory comprising three 16x4 RAMs. The last 15 load pulses are vertical loads. The buffer storage memory RAMs are inhibited from accepting data during the last eight of the counts by the $\overline{\text{DE}}$ command decoded from the 1-of-24 load converter.

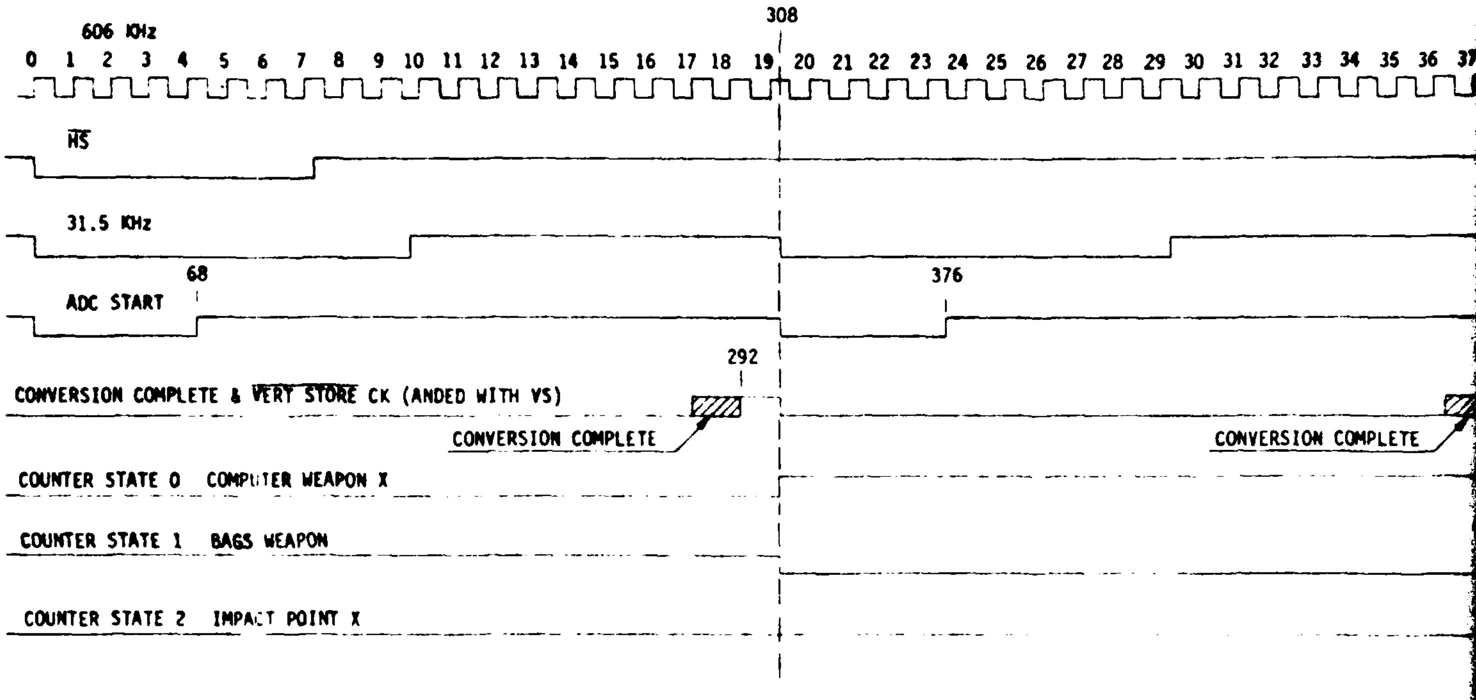
During horizontal blanking the 1-of-24 load counter is clocked at 1.2 MHz. During this interval the data is read out of buffer storage memory RAMs and broadcast as BUFFERED DATA bits 0 through 10.

Impact point vertical data is also on the BUFFERED DATA lines, except that it is used during vertical blanking like the other vertical loads.

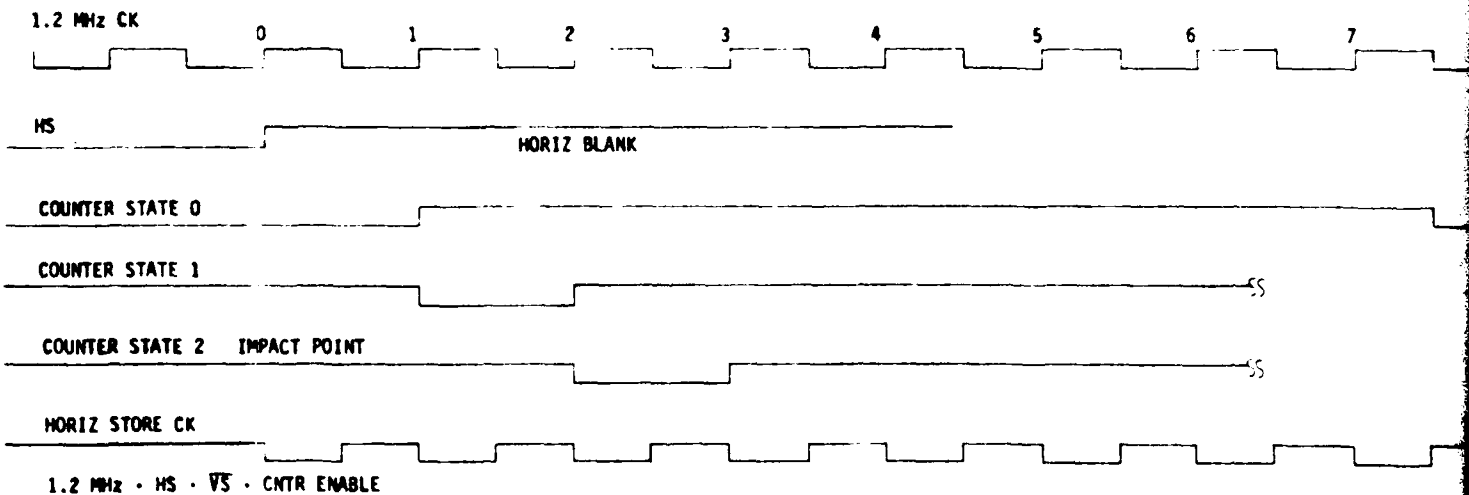
Figure 1-23 shows the counter timing for vertical and horizontal modes.

- Altitude Scale Thermometer. Two altitude scale ROMs are fed with ADC data $\overline{\text{AD2}}$ through $\overline{\text{AD10}}$. The outputs of these ROMs are preset into two counters by the $\overline{\text{ATVL}}$ vertical load pulse from the symbol generator load logic.

Two of the counters are inhibited until the first altitude tick mark is reached, then enabled until they reach terminal count. This means that for 0 feet, all 1's are preset into the counters.



VERT - ADC TIMING 0.412 μSEC/DIV



HORIZ GENERATOR TIMING 0.041 μSEC

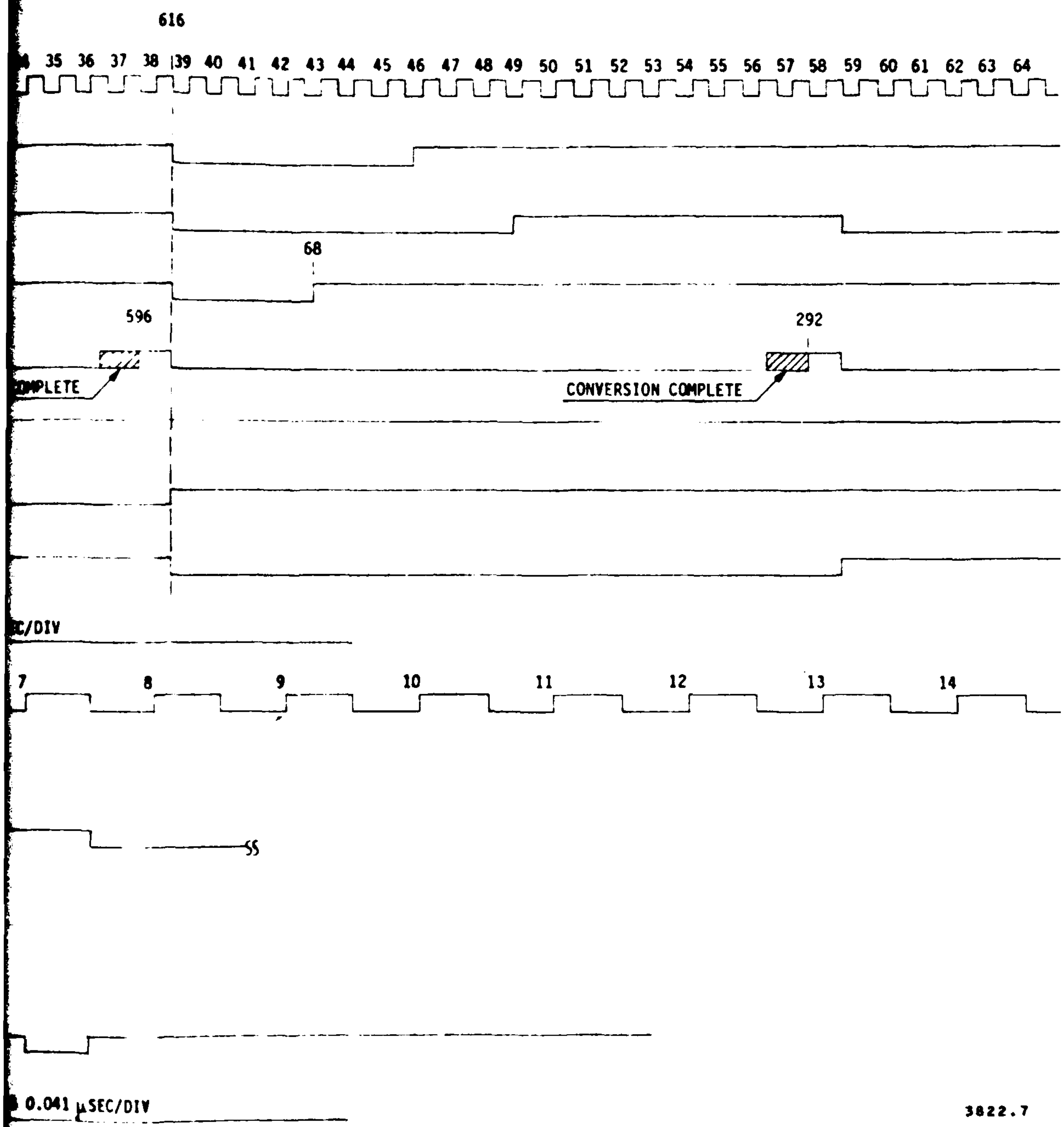


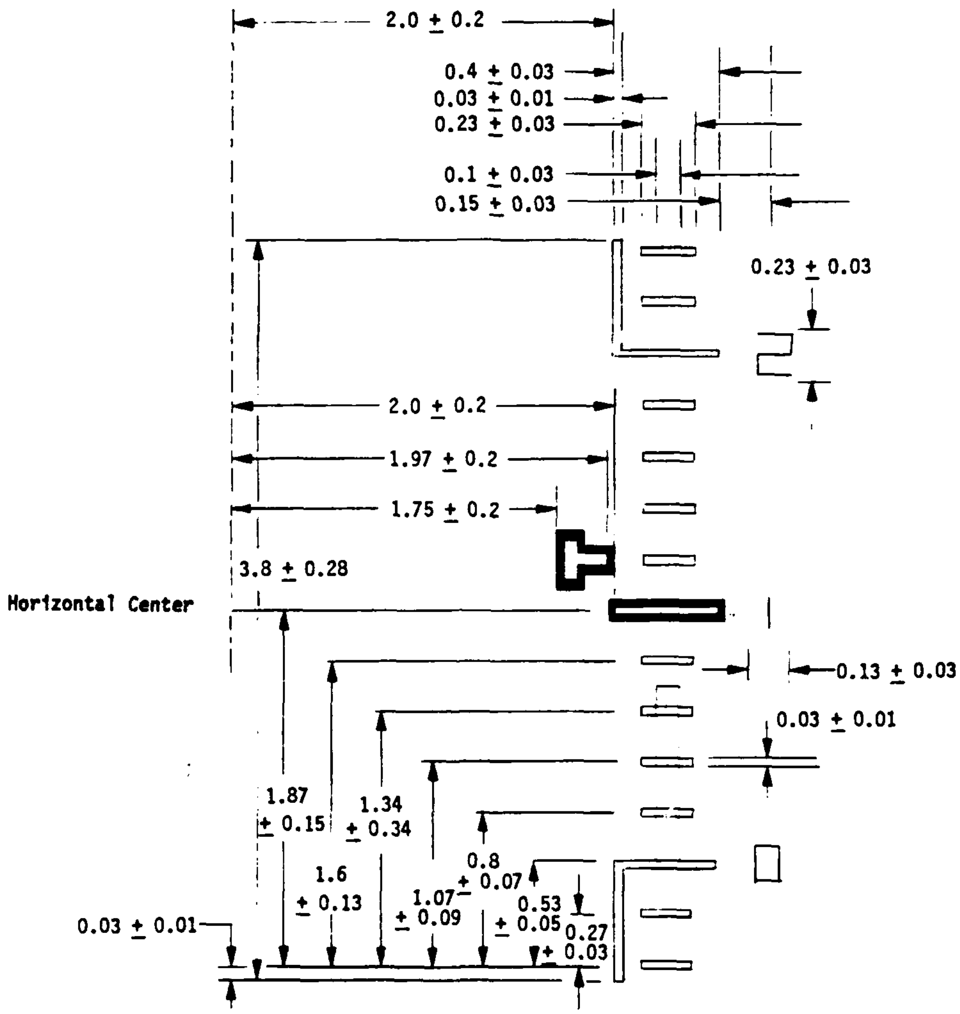
Figure 1-23. AD Conversion Timing

The structure of the ADC 0-10 data (table 1-5) is such that, for all 0's, the thermometer terminates at 400'. For positive data above 400' the ratio is 10 feet per bit. Below 400' the data is negative, decreasing from all 1's slightly below 400'. In that direction the ratio is approximately one foot per bit; 0 feet occurs with input data of -307_{10}.

Table 1-5. Altitude Scale Input Data Structure

Input AD_0-AD_{10}	Feet
0_{10}	400'
10_{10}	500'
60_{10}	1000'
110_{10}	1500'
160_{10}	2000'
260_{10}	3000'
360_{10}	4000'
460_{10}	5000'
0_{10}	400'
-76_{10}	300'
-154_{10}	200'
-230_{10}	100'
-370_{10}	0'

Figure 1-24 shows the number of lines the tick marks are from the 0' tick mark. The ROM output is 511 minus the number of lines [illegible] minus 256; 256 is subtracted since the MSB of the altitude [illegible] always preset at 1, and is not a ROM output.



Notes:
1. Radar scale numerals centered about their approximate tick within ±0.08 inches.
2. All numerics equal in size with a nominal line width of 0.03 inches.

3806.7

Figure 1-24. Radar Altitude Scale — Position of Tick Marks

The ROMs are set up such that thermometer movement between tick marks is approximately linear. The reason for this approach, as opposed to logarithmic, is that logarithmic does not produce a continuous slope between different regions; the linear method provides a smoother slope.

• ROM Programming of Altitude Scale Thermometer. Figure 1-25 shows the calculations used to program the altitude scale ROMs. The ROMs are addressed in the normal manner e.g., $\overline{AD2}$ = address LSB and $\overline{AD10}$ = address MSB.

The tick mark ROM generates tick marks and determines where a number is to appear; because the information for four quadrants is identical, only one ROM is needed. Table 1-6 summarizes the ROM program. The ROMs output the binary value for the numbers to be displayed.

• Magnetic Heading Scale. The input to the magnetic heading scale generator is SDC 0-10 from the synchro-to-digital converter on board 4. When the data is all 0's, 00 should be displayed centered on the index markers. Resolution is 2048 bits per 360°.

Table 1-6. Tick Mark Programming

Feet	Input Bit Range	Lines From 0' Tick	Address	Output
500'	10	50	506	205
1000'	59-61	82	481-482	173
1500'	109-111	110	456-457	145
2000'	158-162	130	431-432	125
3000'	258-262	164	381-383	91
4000'	358-362	194	331-333	61
5000'	458-462	212	281-283	43

LINE 39 - 400'

NOW LINES 4-48 ARE FOR 0' - 500'   35 LINES

48 - 4 = 44 LINES   LINE 3 -

- 0'

400' = 0.8 (44) = 36 LINES $y = 36 - 0.114X$

FEET RANGE	BIT RANGE	CALC FOR SCALE FACTOR	LINES = BITS IN X SCALE FACTOR + BIT LOWER
0' - 400'	0 TO -307_{10}	$\frac{36}{295} = 0.1222$	= 36 - 0.1222 X INPUT BIAS

SCALE FACTOR

300' = -76.8 BITS
200' = -153.5 BITS
100' = -230.3 BITS

INVERTED DATA FROM ALL 1'S.

NOW 1023 - (1023 - BITS) = ROM ADDRESS IF ROM ADDRESS HAD THE USUAL ORDER.

SINCE MSB OF COUNTER IS PRESET.

511 - 256 - LINES = 255 - LINES = ROM OUTPUT

NOW LINES = 39 - 0.114 (BITS)

BITS = 1023 + 2 (ROM ADDR.)

LINES = 39 - 0.114 (2 ADDR.)

30 ROM OUT (USUAL ADDR ORDER) = 255 - 39 + 0.114 (2 ADDR)

0-400' $\boxed{\text{ROM OUT} = 216 + 0.244 \text{ ADDR.}}$

Figure 1-25. ROM Altitude Calculations (0-400') (Sheet 1 of 3)

ROM ALTITUDE CALCULATIONS - OVER 400'

$b_1 \ \ell_1$ —— 3000'

lines y

$b_0 \ \ell_0$ —— 2000'

INP. IN BITS A_0 = LSB

$$\text{SCALE FACT} = \frac{\ell_1 - \ell_0}{b_1 - b_0} (X - b_0) + \ell_0$$

$$\text{ROM OUTPUT} = 511 - 256 - \text{LINES} = 255 - \text{LINES}$$

$$\text{ROM OUTPUT} = 255 - \text{s.f.} (x - b_0) - \ell_0$$

$$\text{BITS} = x = 1023 - 2 \text{ (ROM ADDR)}$$

$$\text{ROM OUTPUT} = 255 - \text{s.f.} (1023 - 2 \text{ ADDR} - b_0) - \ell_0$$

$$\boxed{\text{ROM OUTPUT} = 255 \underbrace{- \text{s.f.} (1023 - 2 \text{ ADDR} - b_0) - \ell_0}_{-\text{ LINES}}}$$

Figure 1-25. ROM Altitude Calculations (0-400') (Sheet 2 of 3)

FEET RANGE	LINE RANGE		BIT RANGE		SCALE FACTOR: $sf = \frac{\ell_1 - \ell_0}{b_1 - b_0}$
	ℓ_1	ℓ_0	b_1	b_0	
400'-500'	48	39	10	0	0.9
500'-1000'	80	51	60	10	0.58
1000'-1500'	108	83	110	60	0.50
1500'-2000'	128	111	160	110	0.34
2000'-3000'	162	131	260	160	0.31
3000'-4000'	192	165	360	260	0.27
4000'-5000'	210	195	460	360	0.15

Figure 1-25. ROM Altitude Calculations (0-400') (Sheet 3 of 3)

The ROM outputs are inhibited to the alphanumeric character generator until the $\overline{\text{HEADING ENABLE}}$ is generated.

- Altitude Scale Numerics. A synchronous counter generates the numbers for the altitude scale thermometer by counting $\overline{\text{MNERTKS}}$ pulses from board 5 during the blanking box of the altitude scale.

- ALS/ILS Decode. The ALS/ILS decode logic generates ALS or ILS code depending on the ALS/ILS mode discrete.

- Character Generator. The alphanumeric character generator ROM is driven by the vertical line counter and the binary data from ROMs which indicate the numeric. Signal BL4 indicates whether it is A, I, L or S. The outputs of the alphanumeric character generator ROM are loaded into a shift register and shifted out as ALPHANUMERIC VIDEO to video mixer board 6.

- Magnetic Heading ROMs. The tick mark ROM contains coding to specify generation of large tick marks, small tick marks, or numeric starts.

The coding is as follows:

	O_4 (HD2)	O_3 (HD1)	O_2	O_1
Large tick	1	1	0	X
Small tick	1	0	0	X
Numeric Start	0	0	1	X

The numeric start code causes the start of a numeric. The numeric is specified by the output of other ROMs.

When all 0's are preset, the display requires 00 and a tick mark to occur at the horizontal center of the screen, as shown below.

0,0

This means that a large tick mark with 00 on either side is required at address 125. One ROM contains a large tick mark at this address, while another ROM gives the 00 information.

For 180° preset SDC10=1 and SDC 9 through SDC0 = 0. For this case the display requires 1,8 to appear in the center. A ROM is addressed and 18 appears such that those characters are centered around the large tick mark at address 125.

- Character Generator ROM. The input addressing of the character generator ROM is:

$$A_7 \quad \underbrace{A_6 \;\; A_5 \;\; A_4 \;\; A_3}_{\substack{\text{CODE} \\ \text{SPECIFYING} \\ \text{CHARACTER}}} \quad \underbrace{A_2 \;\; A_1 \;\; A_0}_{\substack{\text{LINE} \\ \text{ADDRESS}}}$$

$$\left.\begin{array}{l} \text{Numeric} = 0 \\ \text{Alpha} = 1 \end{array}\right\}$$

When $A_7 = 0$, $A_3 - A_6$ specify the numeric to be displayed. The code of $A_6 - A_3$ for the numerics is the binary value of the numeric, inverted, so the code for 2 is 1101. When $A_7 = 1$, and A_5 and A_6 are 1, A, I, L, or S is displayed, dependent on the code for A_4 and A_3:

$$A_7 = 1 \text{ and } A_5, A_6 = 1$$

A_4	A_3	Alphanumeric to be Displayed
0	0	S
0	1	L
1	0	A
1	1	I

A_2 - A_0 are the line address with address 0 at the bottom of the character and address 7 at the top.

1.5.4.5 BOARD 4 (SCHEMATIC 32041). Board 4 contains the hybrid synchro-to-digital converter and the circuitry required to generate and slew (rotate) the command heading lines within the flight path.

Figure 1-26 shows the overall organization of the board. The inputs to this board consist of analog inputs from the flight-path board, digital inputs from the A-to-D converter and symbol control logic, and synchro inputs from the heading synchro transmitter.

A rate latch loads and stores the 9-bit command heading line rate information from the central data bus (ADC lines).

The rate clock generator converts the stored data to a variable-speed clock (maximum frequency 60 Hz).

The rate counter converts the rate clock into a variable-speed 8-bit word. The lowest six bits are used by all the multiplying digital-to-analog converters (DAC's). The largest two bits are offset by fixed offset adders for three of the DAC's. This allows the DAC's to multiply at 90-degree offset intervals.

A vertical mixer provides a combined path clipper/path pull-up 60 Hz sawtooth waveform to the analog input of the DAC's.

The outputs from the DAC's are converted into raster-line video by the symbol generators and mixed together to provide the CHL video output.

A horizontal mixer provides a combined horizontal/near turn/far turn sawtooth waveform to position the command heading lines horizontally on the display.

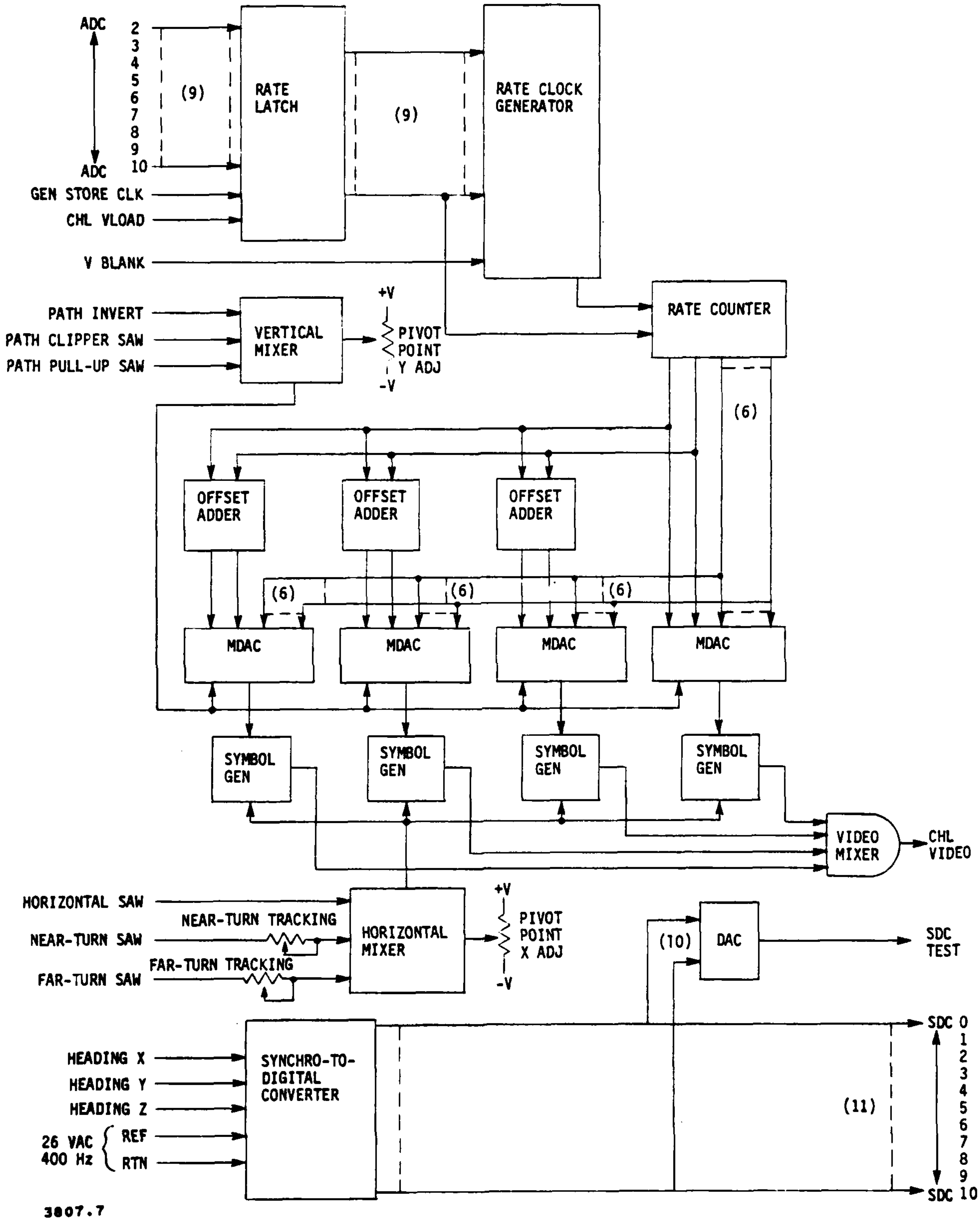


Figure 1-26. Board 4 Block Diagram

The synchro-to-digital converter (SDC) converts the 3-wire heading input to an 11-bit digital output (SDC lines). A fifth DAC combines the major 10 bits from the SDC to provide one test point output.

The following paragraphs present detailed descriptions of the various operations described above.

- Command Heading Lines. The ADC data from board 1 is set up such that when it is all 0's the command heading lines stand still. When the data ADC 2-10 has MSB=0 and the rest all 1's the command heading lines rotate to the right at 2.45"/second. When the data is all 1's the CH lines rotate to the left at 2.45"/second.

Between these maximum and minimum rates, the command heading lines rate increases linearly with the ADC data.

The data is stored in latches during CHL vertical load interval. If the MSB of the data is 0, indicating a positive number, the data is inverted by exclusive OR gates. If the MSB of the data is 1, the data is passed straight through the exclusive OR gates.

Rate clock generators are clocked by GENERATOR STORE CLOCK, which generates more than 16 pulses during every vertical blanking, thus the rate clock generator is preset before VERTICAL BLANKING. During VERTICAL BLANKING, the rate clock generator is clocked until it reaches terminal count, at which time the rate clock latch is reset and the clocks are shut off until the next VERTICAL BLANKING. Because the data preset into the rate clock generator is inverted data, the number of clocks allowed through is proportional to the ADC data value.

The output of the rate clock latch runs two rate counters, which feed four multiplying D-to-A converters.

The maximum rate of the CHL can be controlled by the preset to the rate clock generator. The rate at which a CHL goes from one side of the flight path to the other is $\frac{1}{60} \cdot \frac{11}{16} \cdot 256 = 2.93$ sec. For a 7" width of the flight path the maximum rate is 2.39"/sec.

A dead band is provided around 0V. This causes the CHL to stop if the inputs are less than ± 0.47 volts. If preset data ADC5 through ADC9 = 1 for negative data and ADC5 through ADC9 = 0 for positive data, then the input voltage is less than ± 0.47V, meaning the data from the rate clock generator gates are 1's. This condition is decoded and stored in the rate clock latch which inhibits further movement of the CHL.

1.5.4.6 BOARD 5 (SCHEMATIC 32051). Board 5 contains the system horizontal and vertical timers and related decoding which generate horizontal sync, vertical sync, and various system clocks. Board 5 also contains the vertical (moving) decodes for the ground texture, and the symbol generator for the movable impact point. Figure 1-27 shows the overall organization of the board.

- Horizontal Timing. The system clock is derived from a 9.702 MHz oscillator which is divided down into two approximately 5 MHz clocks, $\overline{\text{CLOCK1}}$ and $\overline{\text{CLOCK2}}$, as shown in figure 1-28. All fixed horizontal timing is derived from the rising edge of $\overline{\text{CLOCK2}}$.

Two counters generate fixed horizontal decodes: the horizontal sync timing counter, and the active line horizontal counter. The horizontal sync timing counter begins counting at the start of horizontal blanking and counts until it terminates, at which time it is disabled.

The active line horizontal counter starts counting at the end of horizontal blanking. When it reaches count 250, it generates a reset decode which restarts the horizontal sync timing counter. At the same time the active line horizontal counter is disabled.

Figure 1-29 shows the relationship of the symbols to the various decodes on board 5.

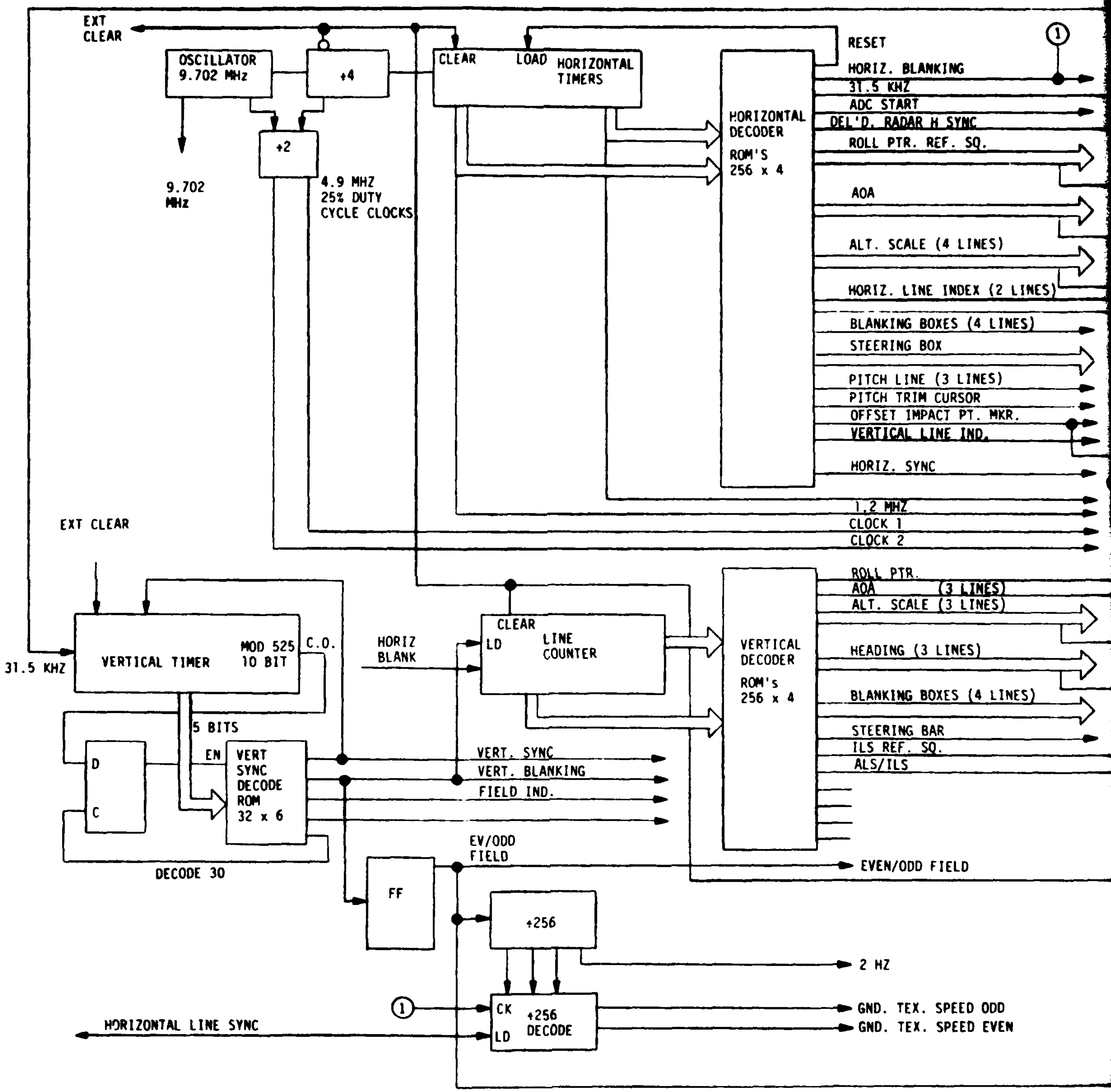
- Vertical Timing. The vertical counter is driven by HVCK which occurs twice per horizontal line. This counter is modulo 525 and generates interlaced vertical sync by virtue of: (1) its odd modulo, and (2) its clock running at twice the horizontal rate.

During 30 of the vertical timer counts a flip-flop is set, enabling the output of a 32x8 ROM to pass through a hex latch to the outputs. Figure 1-30 shows the vertical timer LSB counts for the ROM addresses. The FIELD INDICATOR pulse occurs only during even fields.

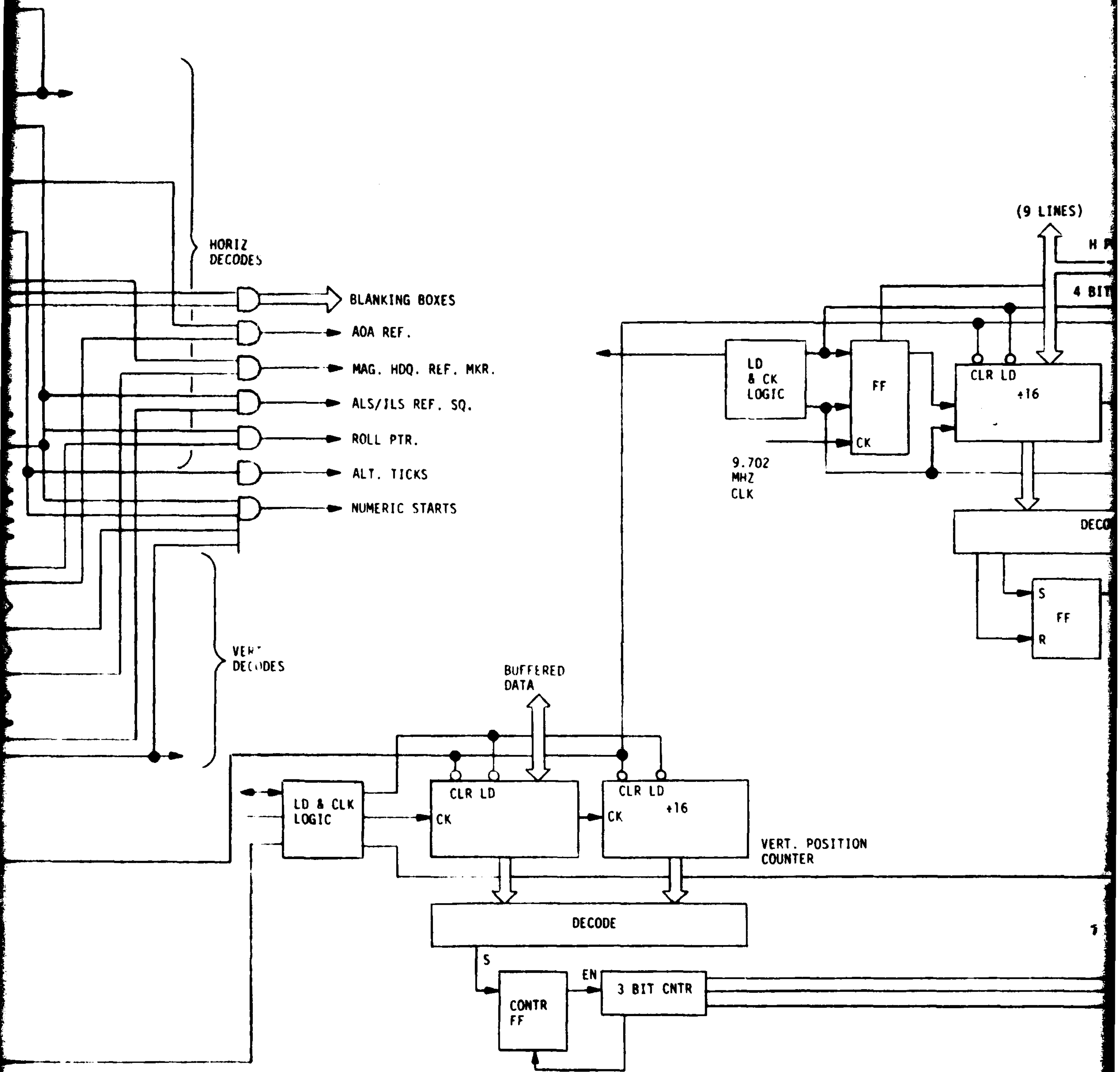
AD-A086 439 KAISER AEROSPACE AND ELECTRONICS CORP PALO ALTO CALIF F/G 17/5
DEVELOPMENT PROGRAM FOR HIGH-RELIABILITY DISPLAY IP-722 (XJ-1)A--ETC(U)
NOV 77 R MULVEY, R SWANTECK, J TISDALE N62269-75-C-0135
UNCLASSIFIED TR-77-100 NADC-75321-36 NL

2 OF 2
AD
A086439

END
DATE
FILMED
8-80
DTIC



EXT CLEAR
OSCILLATOR 9.702 MHz
÷4
÷2
9.702 MHz
4.9 MHZ 25% DUTY CYCLE CLOCKS
CLEAR
LOAD
HORIZONTAL TIMERS
RESET
HORIZONTAL DECODER ROM'S 256 x 4
HORIZ. BLANKING
31.5 KHZ
ADC START
DEL'D. RADAR H SYNC
ROLL PTR. REF. SQ.
AOA
ALT. SCALE (4 LINES)
HORIZ. LINE INDEX (2 LINES)
BLANKING BOXES (4 LINES)
STEERING BOX
PITCH LINE (3 LINES)
PITCH TRIM CURSOR
OFFSET IMPACT PT. MKR.
VERTICAL LINE IND.
HORIZ. SYNC
1.2 MHZ
CLOCK 1
CLOCK 2
EXT CLEAR
31.5 KHZ
VERTICAL TIMER
MOD 525 10 BIT
C.O.
5 BITS
D
C
EN
VERT SYNC DECODE ROM 32 x 6
DECODE 30
HORIZ BLANK
CLEAR
LD
LINE COUNTER
VERTICAL DECODER ROM's 256 x 4
ROLL PTR.
AOA (3 LINES)
ALT. SCALE (3 LINES)
HEADING (3 LINES)
BLANKING BOXES (4 LINES)
STEERING BAR
ILS REF. SQ.
ALS/ILS
VERT. SYNC
VERT. BLANKING
FIELD IND.
EV/ODD FIELD
EVEN/ODD FIELD
FF
÷256
2 HZ
1
CK
LD
÷256 DECODE
HORIZONTAL LINE SYNC
GND. TEX. SPEED ODD
GND. TEX. SPEED EVEN



HORIZ DECODES
BLANKING BOXES
AOA REF.
MAG. HDQ. REF. MKR.
ALS/ILS REF. SQ.
ROLL PTR.
ALT. TICKS
NUMERIC STARTS
VERT DECODES
BUFFERED DATA
LD & CLK LOGIC
CLR LD
CK
CLR LD
÷16
CK
VERT. POSITION COUNTER
DECODE
S
CONTR FF
EN
3 BIT CNTR
(9 LINES)
4 BIT
LD & CK LOGIC
FF
CK
9.702 MHZ CLK
CLR LD
÷16
S
FF
R

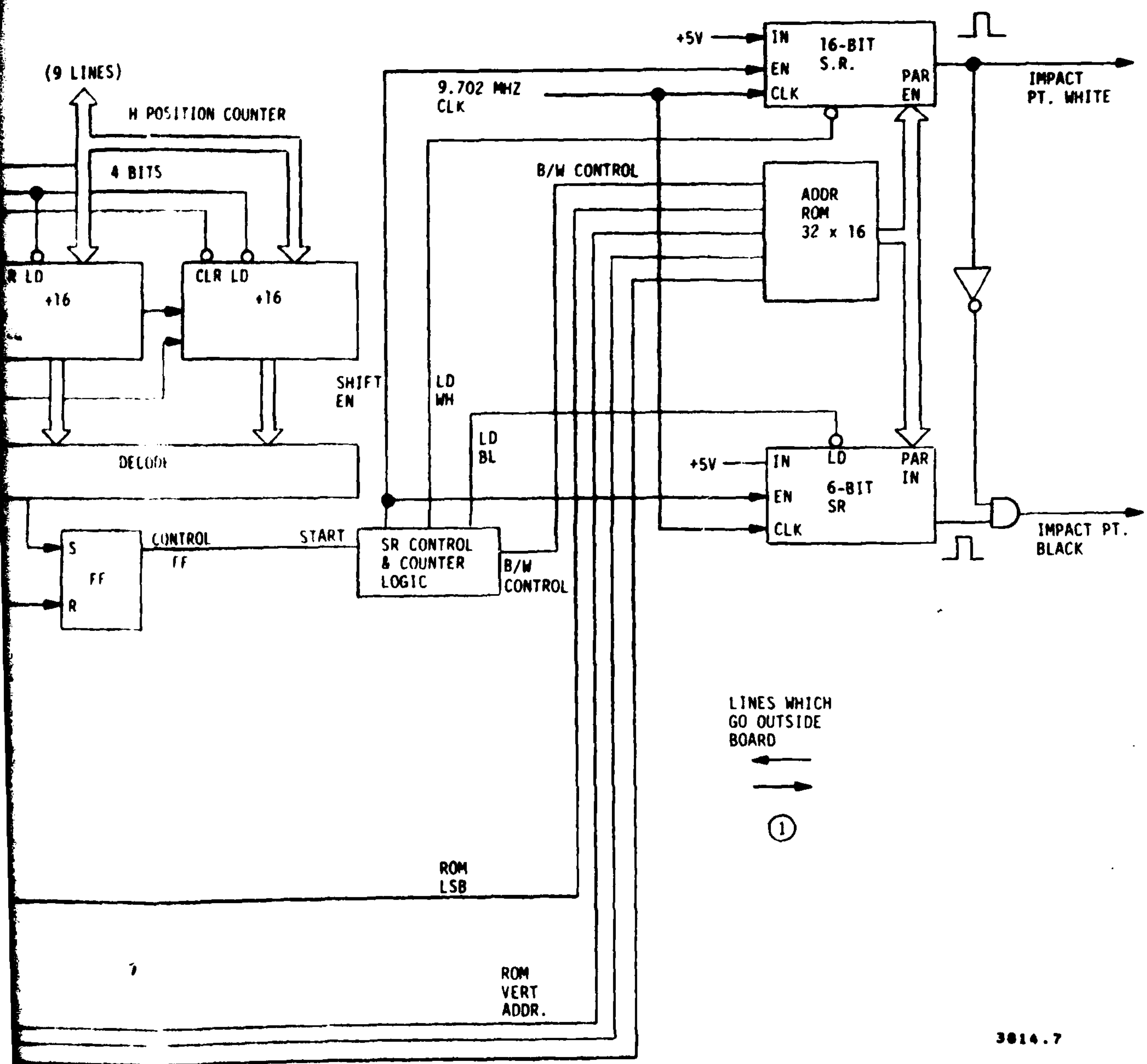


Figure 1-27. Board 5 Block Diagram

3

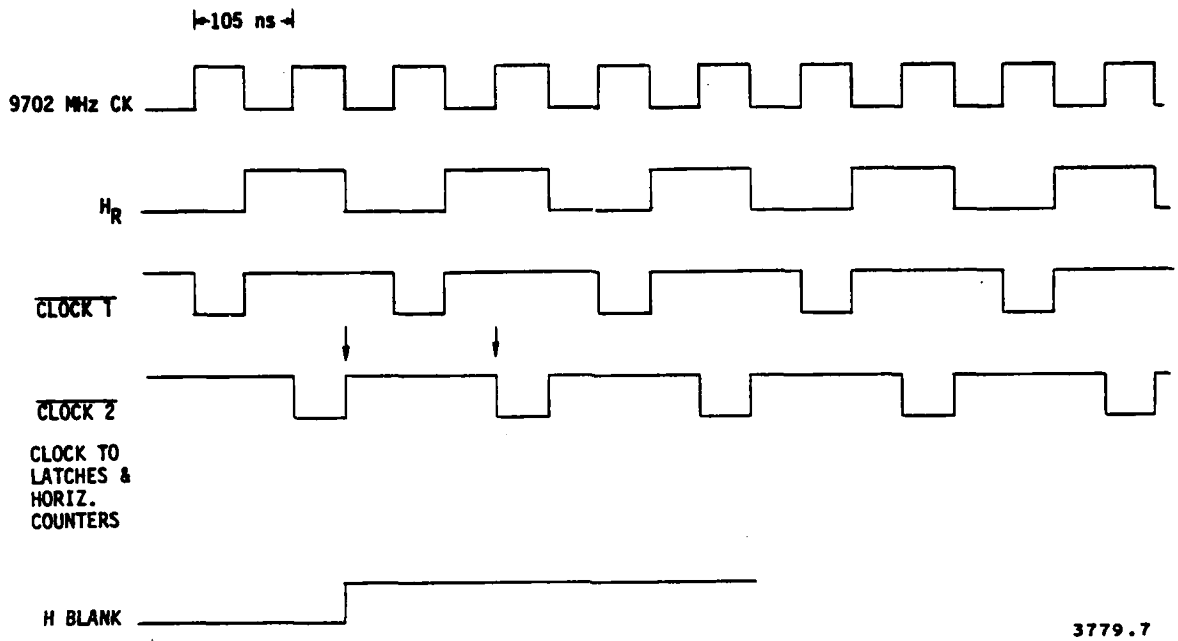


Figure 1-28. Horizontal Detail Timing

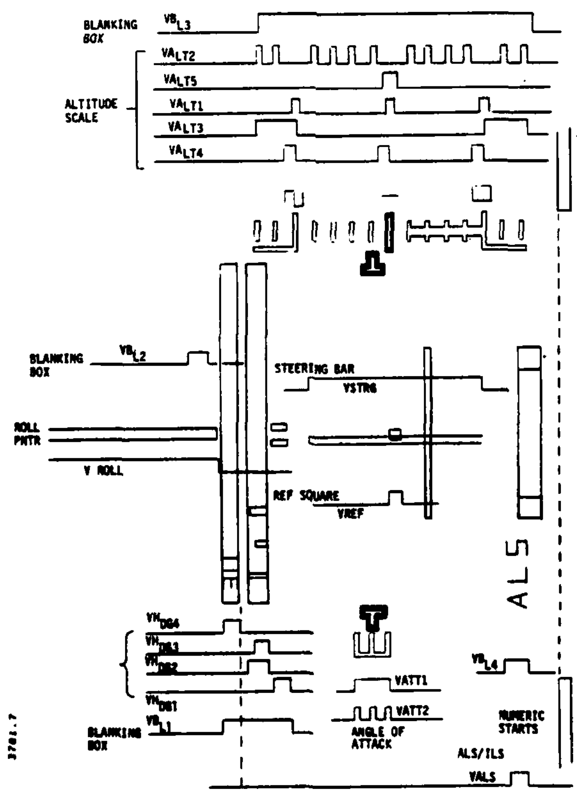


Figure 1-29. Vertical Timing

- Line Counter. Other fixed vertical decoding is generated from a line counter which clocks on the trailing edge of horizontal blanking.

- Ground Texture Vertical Decode. Two fast counters driven from a 30 Hz clock, and two slow counters clocked on horizontal blanking, are decoded to form the ground-texture vertical decodes. At the time the horizon is present, these counters are preset with the count in the slower counters. Figure 1-31 shows some of this timing.

FIELD INDICATOR clocks the slow counters during even fields. This allows the decodes to move down one line per frame.

As a result, the rate at which the decodes move down the screen is determined by the fast counters, while the size and interval of the decodes is determined by the slow counters. The decodes thus move down the screen and appear locked to the horizon line when the horizon moves up and down.

- Impact Point. Because the impact point is a circle, more resolution was needed for it than for other symbols; it has a 10 MHz horizontal resolution and a one-line vertical resolution. The symbol is formed by a character generator. The counters count until they reach a particular decode which locates the symbol. The contents of 32x8 character generator ROMs are then loaded into shift registers and shifted out.

- Impact Point Vertical Counter. The impact point vertical counter is preset with data during vertical retrace, and clocked by HORIZ BLANKING during the active vertical period. The vertical LSB position is obtained from BUFFERED DATA BIT 2. When this bit is 1, a clock pulses the counter in the even field, but not the odd field, allowing the symbol to move down the screen one line per frame.

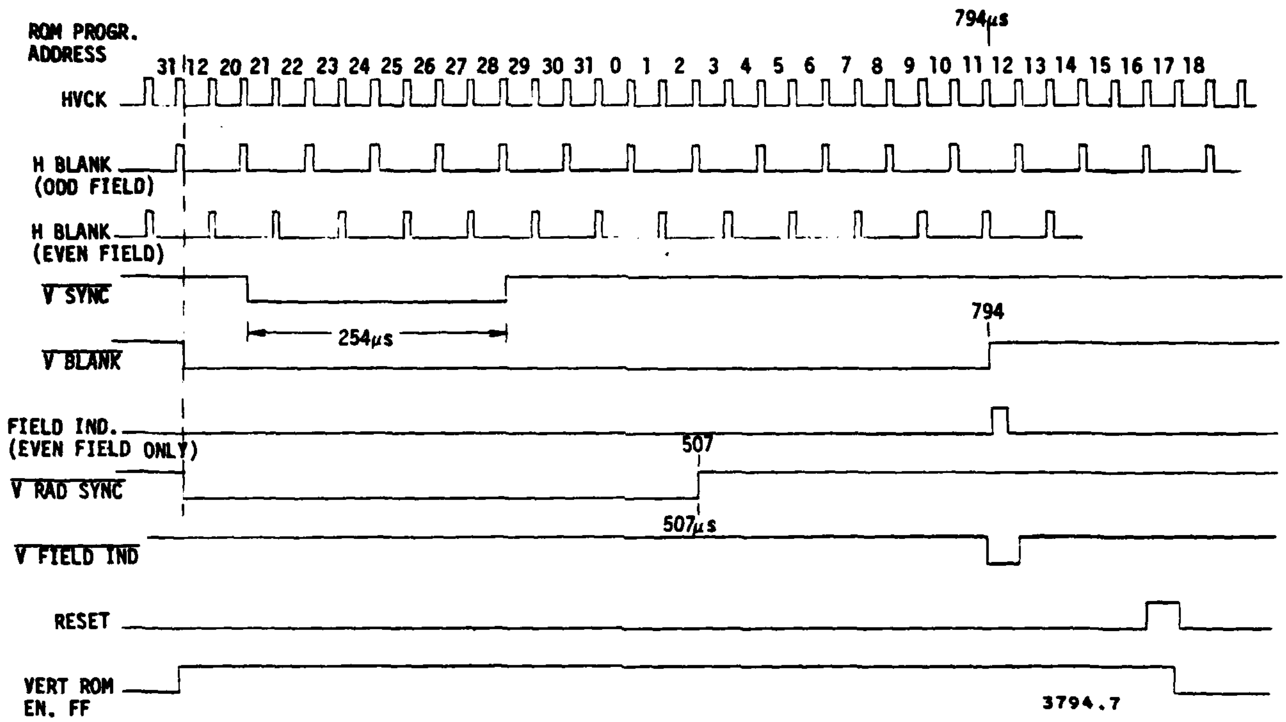


Figure 1-30. Vertical Timer Decoding

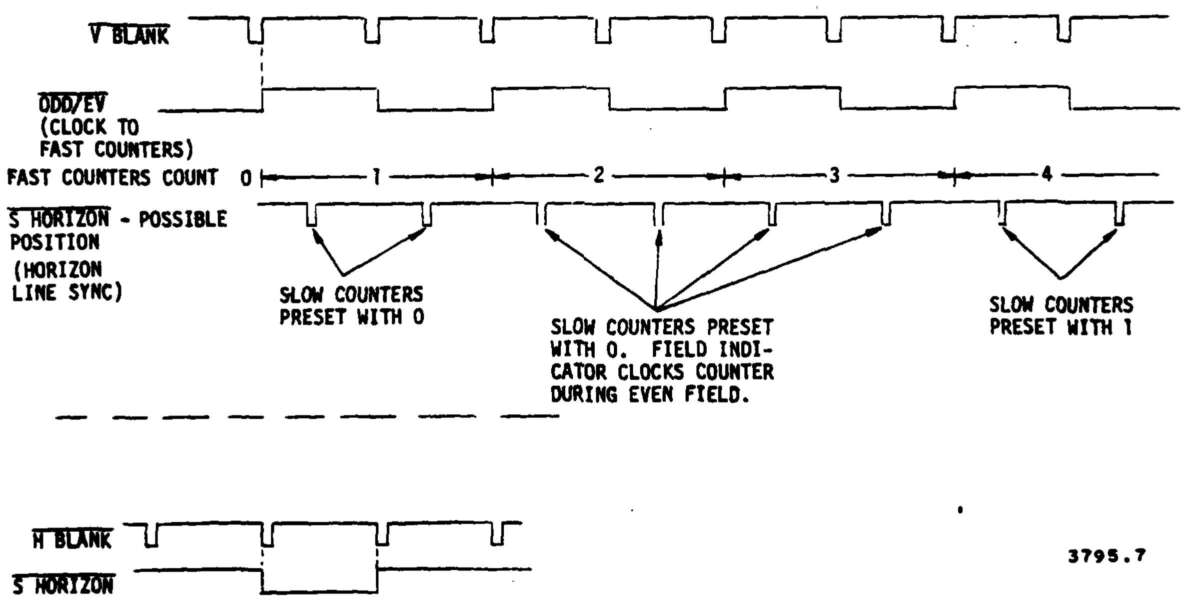


Figure 1-31. Ground Texture Vertical Decode Timing

Figure 1-32 shows the timing involved. The symbol enable flip-flop is high during the eight lines/field that the symbol is displayed.

- Impact Point Horizontal Counter. The impact point horizontal counter is preset during horizontal retrace and clocked by the 10 MHz clock as shown in figure 1-33.

At decode 236, the white shift register is loaded with white data from a ROM. Similarly, at decode 238 the black shift register is loaded with black data from the ROM.

When symbol enable Y flip-flop is high, symbol start X flip-flop is allowed to set on the proper decode. This allows shifting out. When all the data has been shifted out, both shift register outputs continue shifting 0's to indicate no symbol.

- Programming of the Impact Point ROMs. Figure 1-34 gives a diagram of the addressing for the impact point ROMs. The symbol is formed from two solid circles from the ROM, a black one and a smaller white one. The black part of the symbol is BLACK DISC $\cdot$ $\overline{\text{WHITE DISK}}$. The white part of the symbol is WHITE DISC. The diagram shows only the final symbol. One ROM contains the left half of the symbol, a second ROM contains the right half. A_4 of the address specifies whether the black disc or white disc is to be output, while A_3 - A_0 specify the line of the symbol to be displayed.

- WRA Test Points. In order to provide WRA testing for all outputs, some signals are multiplexed. TP-AA contains a number of vertical outputs multiplexed horizontally. TP-HH and TP-FF contain horizontal outputs multiplexed vertically. Viewing these on the monitor provides a simple method of checking these and other test points.

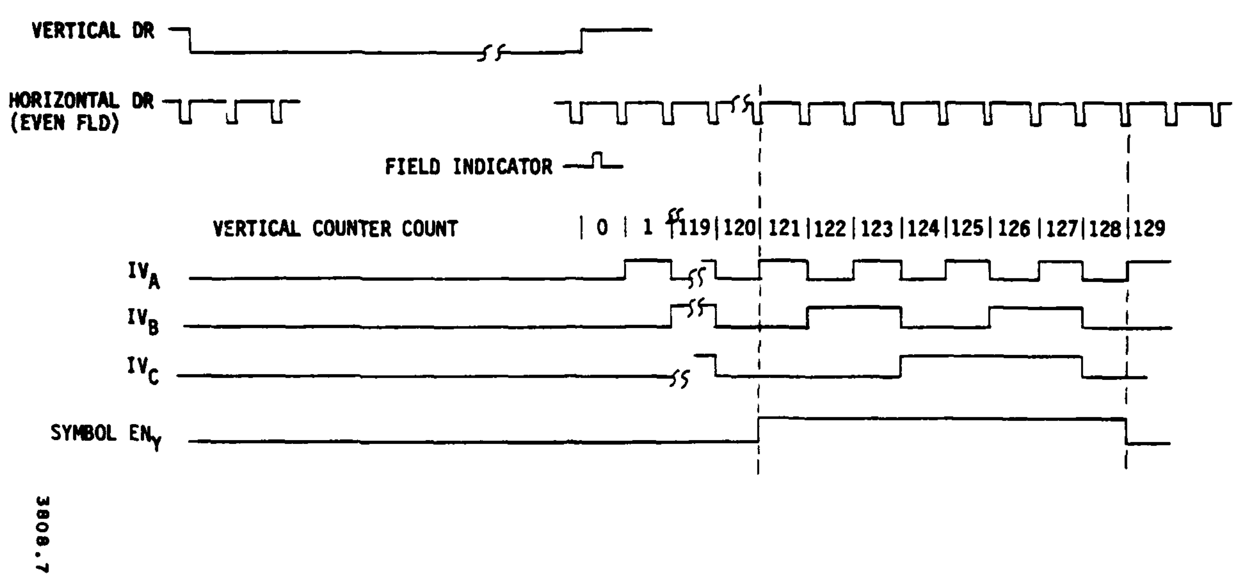
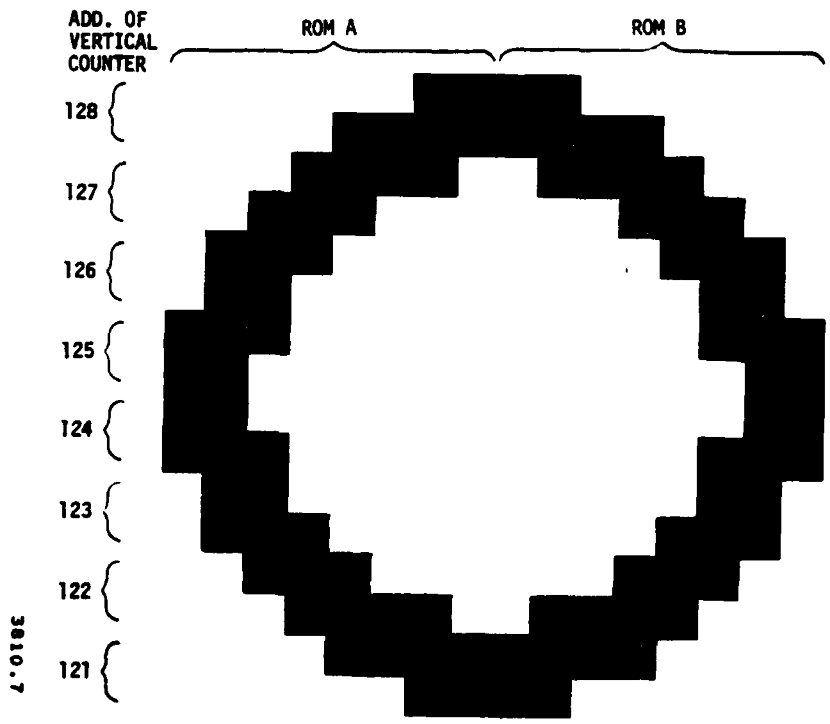


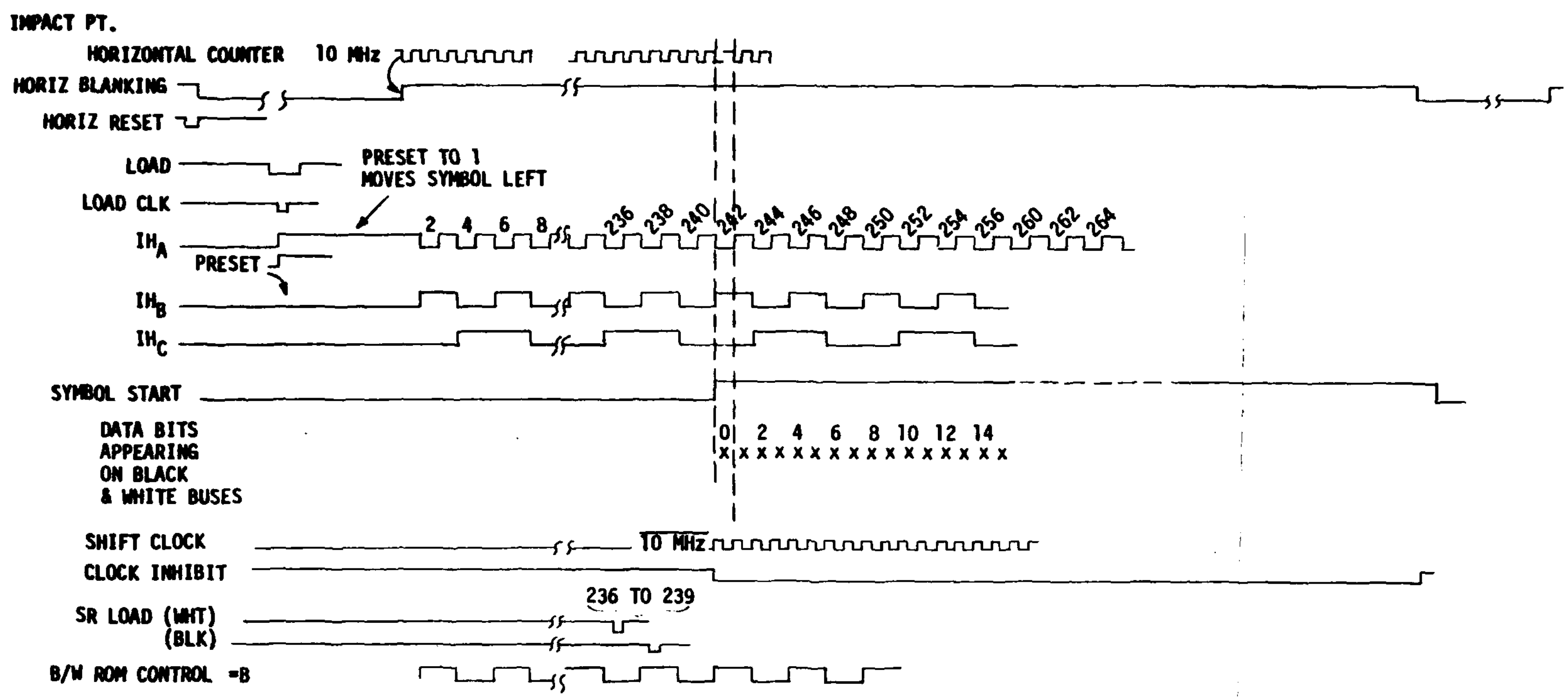
Figure 1-32. Impact Point Vertical Counter Timing



ROM ADDRESSES:

BLACK	WHITE
16	0
17	1
30	14
31	15
28	12
29	13
26	10
27	11
24	8
25	9
22	6
23	7
20	4
21	5
18	2
19	3

Figure 1-33. Impact Point ROM Addressing



	I	M	G	F	E	D	C	B	A
236	0	1	1	1	0	1	1	0	0
	0	1	1	1	0	1	1	0	1
238	0	1	1	1	0	1	1	1	0
	0	1	1	1	0	1	1	1	1
240	0	1	1	1	1	0	0	0	0
241	0	1	1	1	1	0	0	0	1
242	0	1	1	1	1	0	0	1	0

3809.7

Figure 1-34. Impact Point Horizontal Counter Timing

1.5.4.7 BOARD 6 (SCHEMATIC 32061). Board 6 performs the following functions:

- Converts timing signals received from symbol generators to shades-of-grey composite TV video.
- Performs mode switching utilizing 28-volt mode and symbol on-off signals received from the aircraft; provides TTL mode information to other subassemblies.
- Receives, selects, and scales video received from the radar data converter and the detecting and ranging set.

Figure 1-35 presents a generalized overview of the video mixing process.

Symbols are divided into 3 groups for logic purposes.

Group 1 Video - Symbols required in contact analog and TC mode

Group 2 Video - Symbols required in contact analog mode only

Radar Video - Symbols required in TC mode only

Symbols with associated on-off signals are not displayed in operational modes unless an "on" signal is received.

In test mode, on-off signals are overridden and symbols turned on. Whether they are actually displayed depends on the group inputs; i.e., Group 1, Group 2, or Radar.

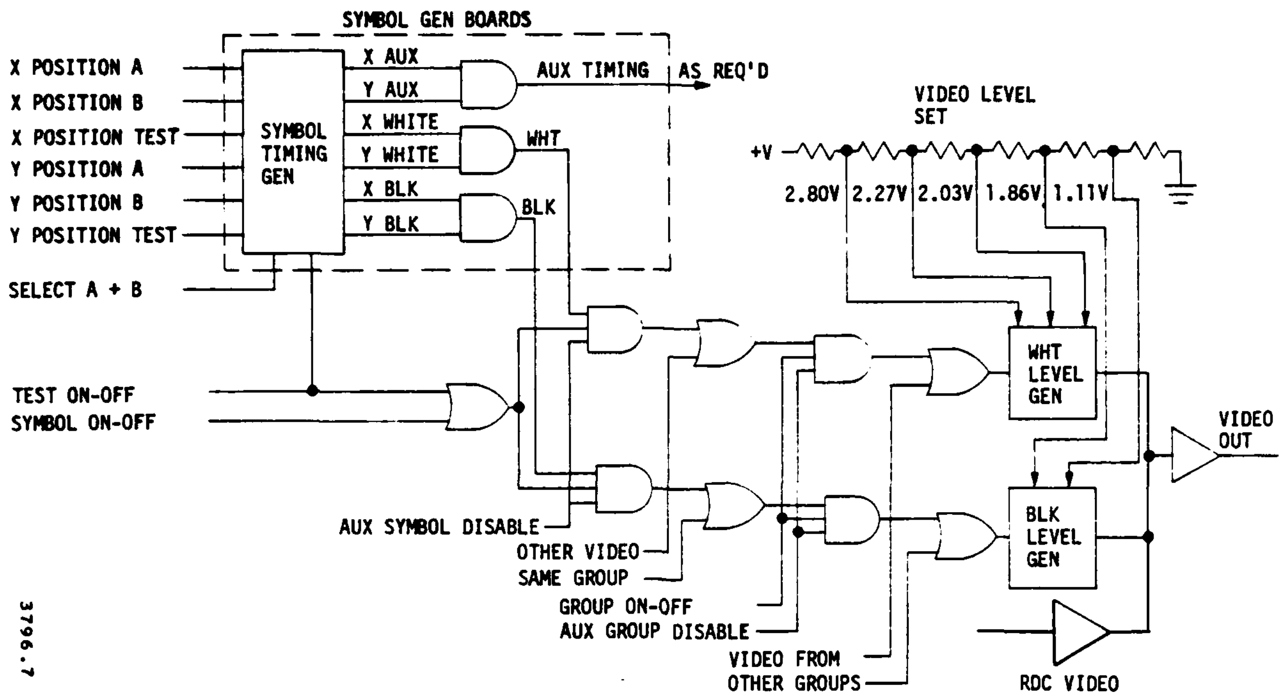


Figure 1-35. Generalized Symbol Video Mixer

On-off and other 0 or 28 Vdc signals may be either at 0 V (externally terminated), or open. 28 Vdc levels are from aircraft 28V which is noisy and can be between 17 and 32 Vdc. Table 1-7 summarizes symbol versus mode constraints.

Table 1-7. Symbol Constraints

SYMBOL	SYMBOL ON-OFF	GROUP 1 ON-OFF	GROUP 2 ON-OFF	RADAR ON-OFF	MISCELLANEOUS
Impact Point		X			Note 2
Target Symbol	X	X			Note 6
Weapon Symbol	Note 3	X			Note 6
Pull-Up Marker	X	X			
Release Marker	X	X			
Flight Path	X	X			Note 6
Path Center Line	Note 4				Note 6
Command Heading Line	Note 4				Note 6
Pitch Lines, $+90^0$, $+60^0$, $\pm 30^0$, -40^0		X			
Roll Pointer		X			
Magnetic Heading Scale		X			Note 5
Angle of Attack Symbol		X			Notes 5,10
Radar Altitude Scale		X			Notes 5,8
ACLS/ILS Steering		X			Notes 5,6
ALS/ILS Alpha		X			Notes 5,6,9
Pitch Trim Cursor		Note 1	Note 1		
Horizon, $\pm 10^0$, $\pm 20^0$ Pitch Lines			X		
Ground/Sky			X		
Offset Impact Point				X	
RDC Video				X	

NOTES:

1. Pitch trim cursor depends on Group 1 on-off if input 33b is present, and Group 2 on-off if input 33b is open.
2. Impact point blinks if stall signal (input 69) is present.
3. Weapon symbol has two on-off's (inputs 14 and 66).

Notes continued

NOTES: (for table 1-7)

4. Path center line or command heading lines are displayed when path is on. Input 2 determines which is displayed.
5. New symbols are not displayed if aircraft identification (input 114) is open. Also, the ACLS/ILS validity (input 105) will not be applied to the target, weapon, and path.
6. Depends on ACLS/ILS validity signal (input 105) if aircraft identification (input 114) is present.
7. Depends on TRAM on-off and CONDOR on-off:

TRAM on-off CONDOR on-off	0 don't care	Mode determined by Group 1, Group 2, radar inputs
TRAM on-off CONDOR on-off	1 0	FLIR mode - FLIR video displayed. Overrides Group 1, Group 2, and radar inputs.
TRAM on-off CONDOR on-off	1 1	CONDOR mode - CONDOR video displayed. Overrides Group 1, Group 2, and radar inputs

8. Radar altitude scale is displayed if aircraft identification (input 114) and altitude reliable (input 5) are present.
9. ALCS/ILS mode signal (input 113) determines whether ALS or ILS is displayed.
10. Landing mode signal (input 112) determines whether angle of attack signal is displayed.

Figure 1-36 shows details of the TC and CA video.

When two symbols overlap, brighter shades override darker shades with the following exceptions:

- All blacks override sky and ground grays
- Impact point, offset impact point, weapon, and target shading (black component) override any lighter shades
- Path bright area is additive with any other video except release and pull-up markers, path outline, center line, and command heading lines, and symbol shading noted above; these override path video.

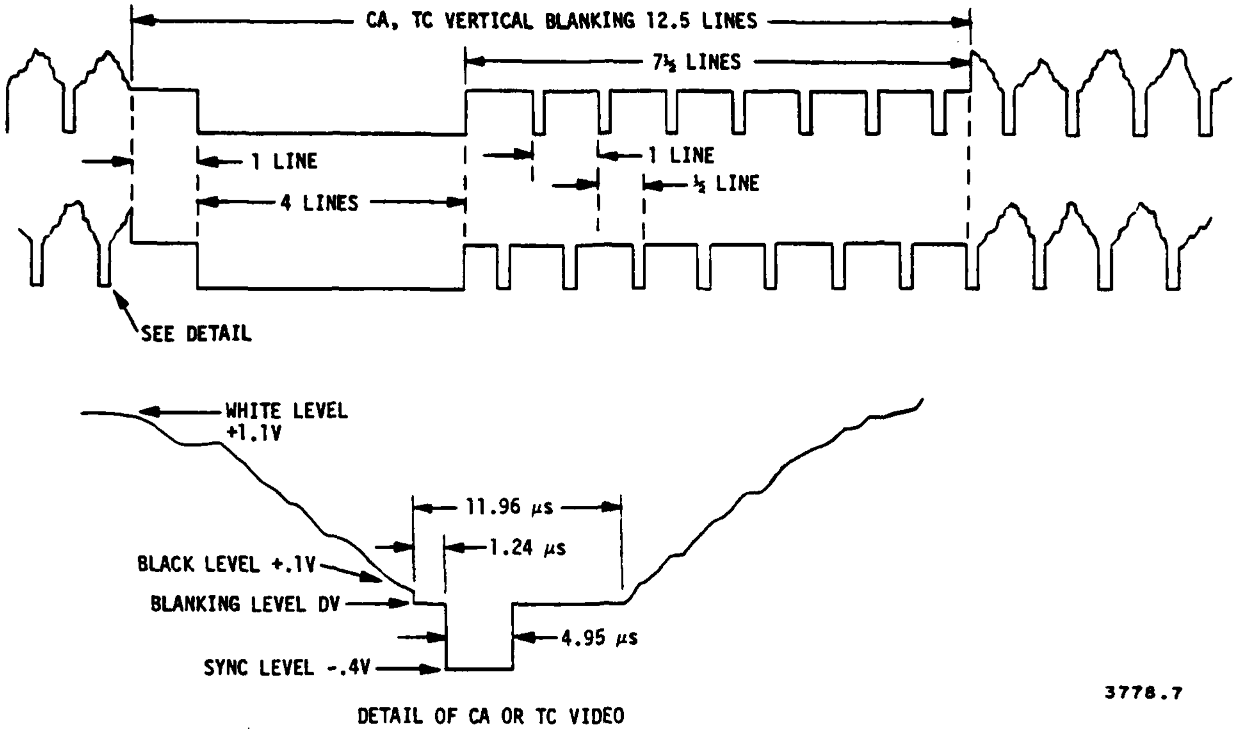


Figure 1-36. Contact Analog or Terrain Clearance Video

1.5.4.8 BOARD 7 (SCHEMATIC 32071). Board 7 generates the following signals:

- Ground texture video.
- Release marker video.
- Pull-up marker video.
- Fixed-amplitude horizontal and vertical rate saw-tooths for use in analog symbol generation.

Figure 1-37 shows the overall organization of the board.

A 31.5 kHz band-pass filter forms a digital square wave into a sine-wave (31.5 kHz fixed phase) for use by an azimuth angle resolver located in the aircraft's inertial navigation system. The output of this resolver (31.5 kHz variable phase) is used for the horizontal positioning of the ground texture. The 31.5 kHz variable phase is buffered, then converted to a triangular wave by a comparator and integrator.

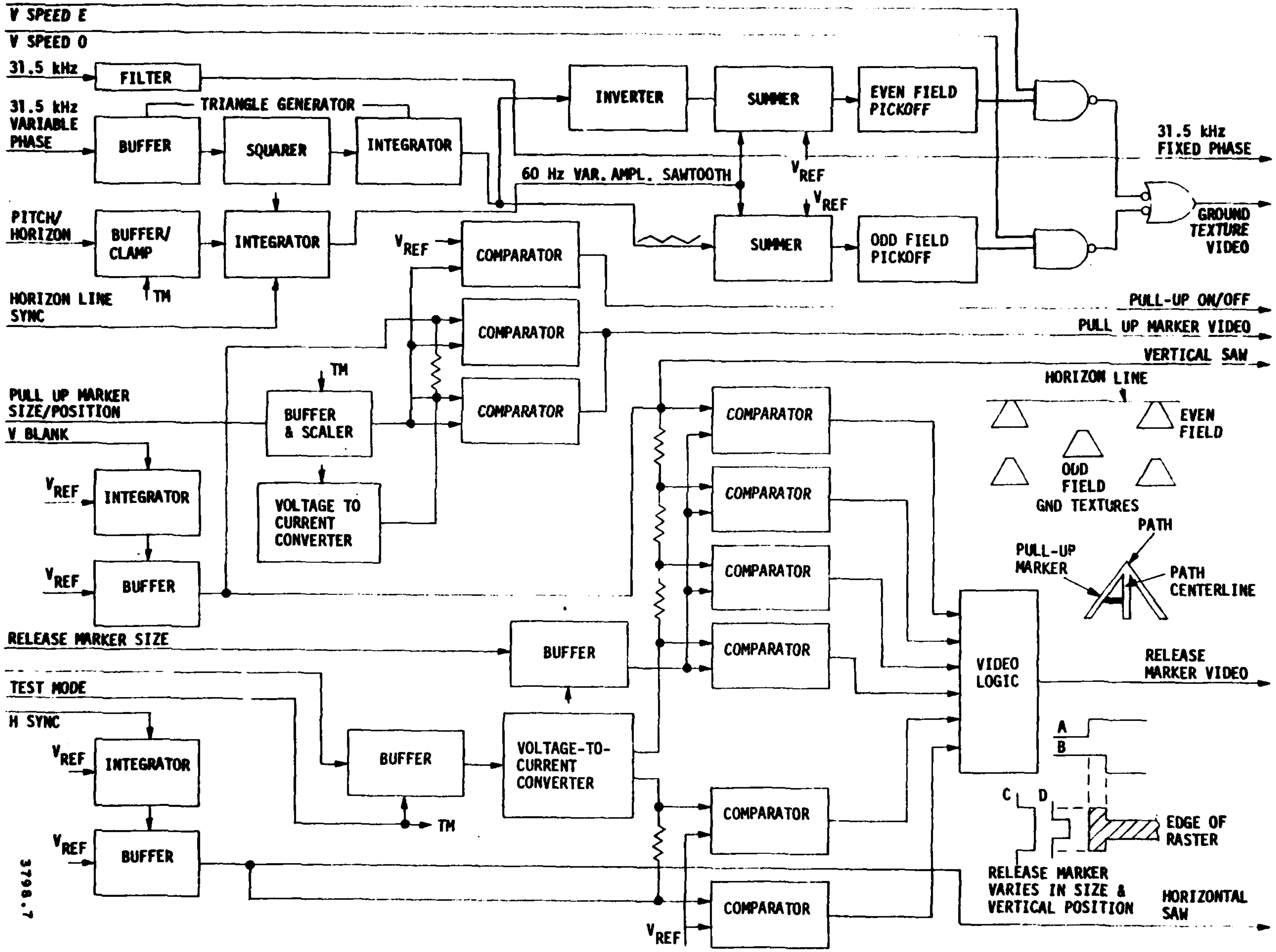


Figure 1-37. Board 7 Block Diagram

The pitch input, used to change the shape of the ground texture elements for pitch angles less than -35° (e.g. -40°), is first buffered and changed such that the buffer/clamp output is zero for all pitch angles greater than -35° (e.g. -25°, +10°). The buffer/clamp output is inverted, summed with an offset voltage and converted to a ramp by an integrator. Thus, for pitch angles greater than -35°, the only voltage contributing to the ramp is the offset voltage. For pitch angles less than -35°, the inverted pitch information is subtracted from the offset voltage resulting in the generation of a smaller ramp. The integrator is reset with HORIZON LINE SYNC. This ramp, which occurs at a vertical sweep rate, is summed with the triangular wave and an offset voltage used to determine the clipping level of the resultant composite waveform. The offset voltage is adjusted so that only the peaks of the triangular wave riding on top of the ramp are converted to horizontal video by the comparator.

This horizontal video is gated with the vertical video (SPEED 1 and SPEED 2) to provide the ground texture video.

The sawtooth generators comprise standard integrator and buffers, providing vertical and horizontal rate sawtooths with outputs corresponding to 1.2 volts/display inch (i.e., 10 VP-P is equivalent to a display size of 8.33 inches).

The pull-up position signal determines the position and size of the pull-up markers, and is fed into a buffer/test mode switch which outputs either the scaled position/size information, or the fixed position test mode information. The output is fed to a voltage-to-current converter which, via a resistor tied between the comparators, generates a window (i.e., symbol size) proportional to the pull-up marker's position. The comparator's open-collector outputs are connected in a wire-AND configuration.

The vertical position of the pull-up marker is such that an input signal of zero volts positions the center of the pull-up marker to within 0.125 inches of display center, and an input of +7.5 Vdc positions the center of the pull-up marker 1.94 ± 0.28 inches below the display center.

The size of the pull-up marker is such that zero volts corresponds to maximum size:

Maximum Size - 0.0V = 0.25 ± 0.06 inch
Minimum Size - +15.0V = 0.12 ± 0.06 inch

The pull-up position signal also provides a command change output at +10 Vdc input to switch the flight path into a pull-up mode.

Generation of the release marker video is conceptually similar to the generation of the pull-up marker video with the exception that position and size information are brought in on two separate lines.

The vertical position of the release marker is such that an input signal of zero volts positions the center of the marker to within 0.12 inch of display center, a +11.8 Vdc signal positions the center of the marker 2.88 ±0.12 inch below the display center.

The size of the release marker is such that zero volts corresponds to maximum size:

Maximum Size - 0.0 volts = 0.25 ±0.06 inch
Minimum Szie - +15.0 volts = 0.12 ±0.06 inch

1.5.4.9 BOARD 8 (SCHEMATIC 32081). Board 8 contains the circuitry required to generate the flight path.

Figure 1-38 shows the overall organization of the board.

The inputs to this board consist of analog and digital inputs controlling the position, size, and shape of the centerline and the flight path.

Input buffers provide common-mode rejection of external ground noise, scale the inputs to the correct amplitudes, and provide fixed test mode voltages.

The sawtooth generators (near-turn, far-turn and path) accept variable dc inputs and generate linear sawtooth waveforms at a 60-Hz rate.

The pull-up function generators (pull-up and inverted pull-up) generate exponential waveforms at a 60-Hz rate to provide the curve in the path during pull-up commands.

The vertical pickoff, one-shots, and keyed clamps provide variable zero (center) positioning for the sawtooths controlling the center line and the flight path. The near-turn sawtooth is clamped slightly above the path apex to allow the command heading line pivot point to be out of view (outside the flight-path border).

The path motion mixer sums the near and far-turn and horizontal sawtooths to provide a field-of-view centerline waveform. The centerline window detector picks off a narrow vertical line at center inside the flight path.

The path "Y" Position Reference switch selects between normal vanishing point vertical position and command altitude control (during pull-up) of the path apex vertical position.

Inverters invert the path and pull-up waveforms to keep the path right-side-up on the display when the roll-angle is greater than $\pm 110^{\circ}$.

The summer amplifier generates the complex horizontal ramp waveforms used to make the basic flight path. The path symbol generator circuitry generates the path outline and also provides the inside area of the path via window detectors.

The positional accuracy of the flight path apex on the horizon line at display center is better than 0.4 percent full scale.

The path altitude switching circuit changes to a pull-up mode when the system pull-up marker position input from board 7 exceeds a preset threshold, at which time the path width (altitude) is switched to the normal size.

The command altitude change input positions the path apex vertically while in the pull-up mode with zero radius of curvature input as follows:

Command Alt. Change	Path Apex Position
0 V	1.3 inches down
+7.5 V	Display center
+15 V	1.3 inches up

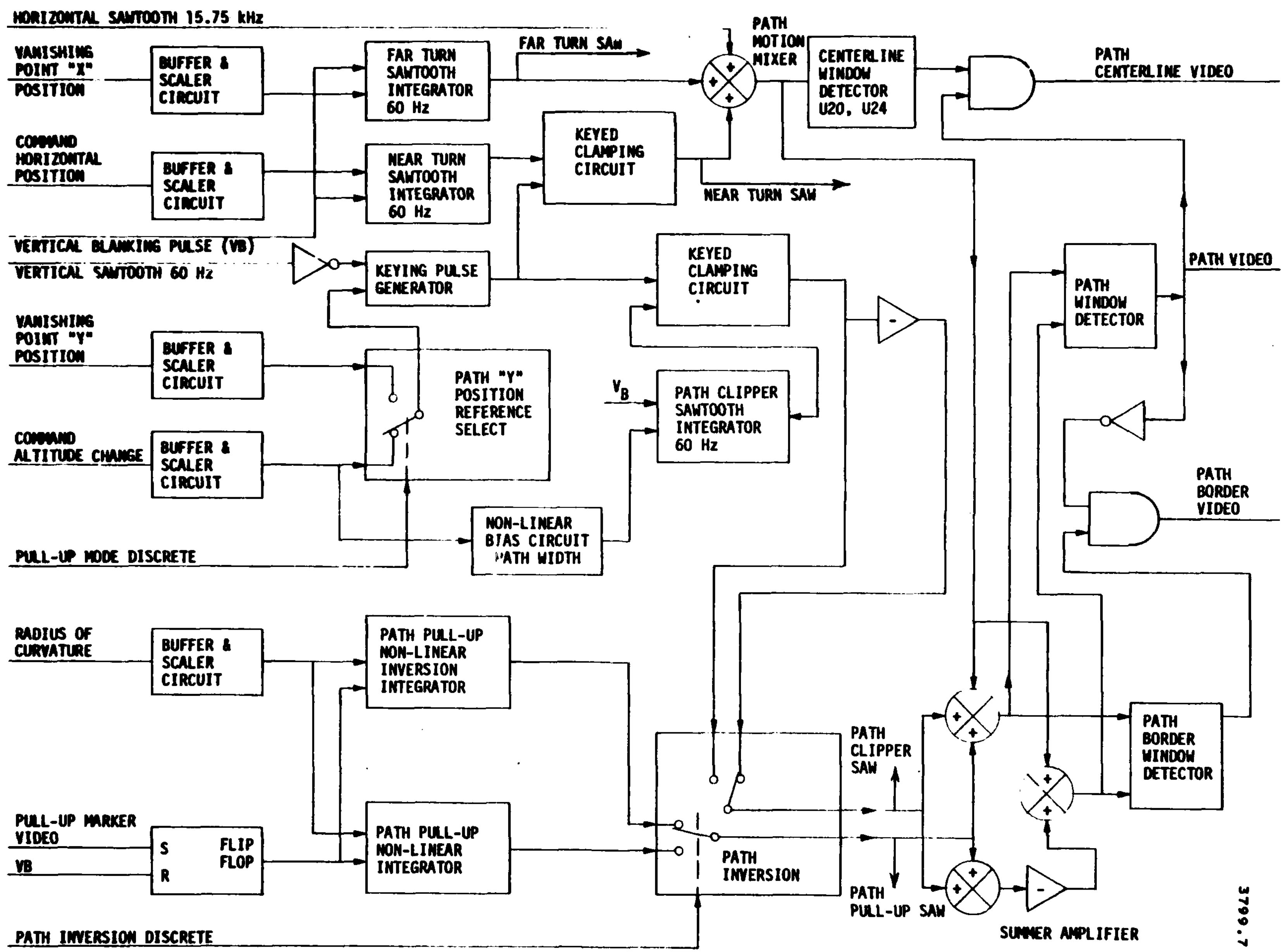


Figure 1-38. Board 8 Block Diagram

1.5.5 Indicator

1.5.5.1 GENERAL. The following paragraphs present detailed descriptions of the indicator SRAs, comprising:

- Line scan deflection
- Field sweep deflection
- Video amplifier
- Roll servo
- LVPS
- HVPS

1.5.5.2 LINE SCAN DEFLECTION (SCHEMATIC 32172). The line scan deflection circuit (LSDC) provides line scan sweep currents to the deflection yoke for the ADI, RDC, FLIR, and CONDOR modes in accordance with the following table:

Mode	Raster Width (Inches)	Line Rate (kHz)	Lines
ADI	8.33	15.750	525
RDC	8.33	15.750	525
FLIR	5.7	44.64	1486
CONDOR	7.6	15.33	511

Figure 1-39 shows the organization of the LSDC. The LSDC is a resonant scan device which recovers flyback energy to conserve power. A line scan size circuit determines the raster size as a function of mode. A line scan centering circuit shifts the raster according to mode in order to keep the center of the sweep at the center of the display. The deflection amplifier generates a sawtooth deflection current, which is synchronized by a phase lock loop drive circuit. A power regulator circuit supplies drive power to the output amplifier and adjusts the supply voltage as a function of mode. The sweep current is inhibited in the absence of line scan sync. Figure 1-40 defines the characteristics of the various sync inputs.

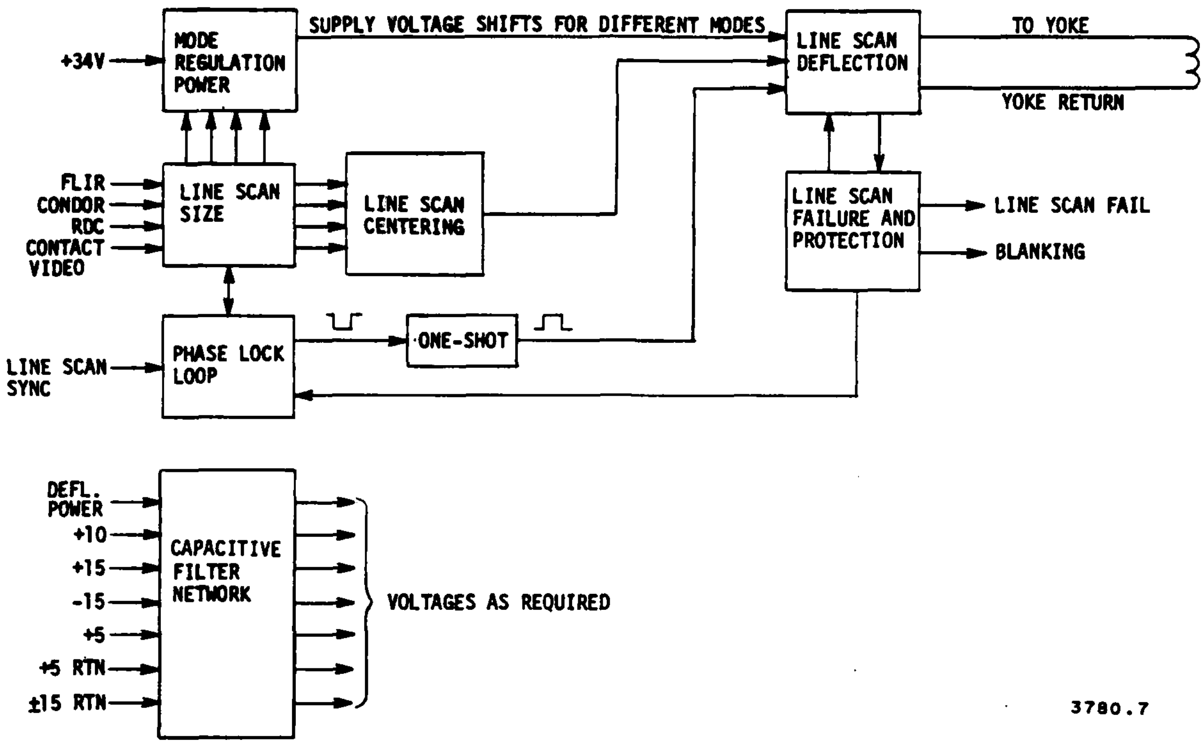


Figure 1-39. Line Scan Detection Block Diagram

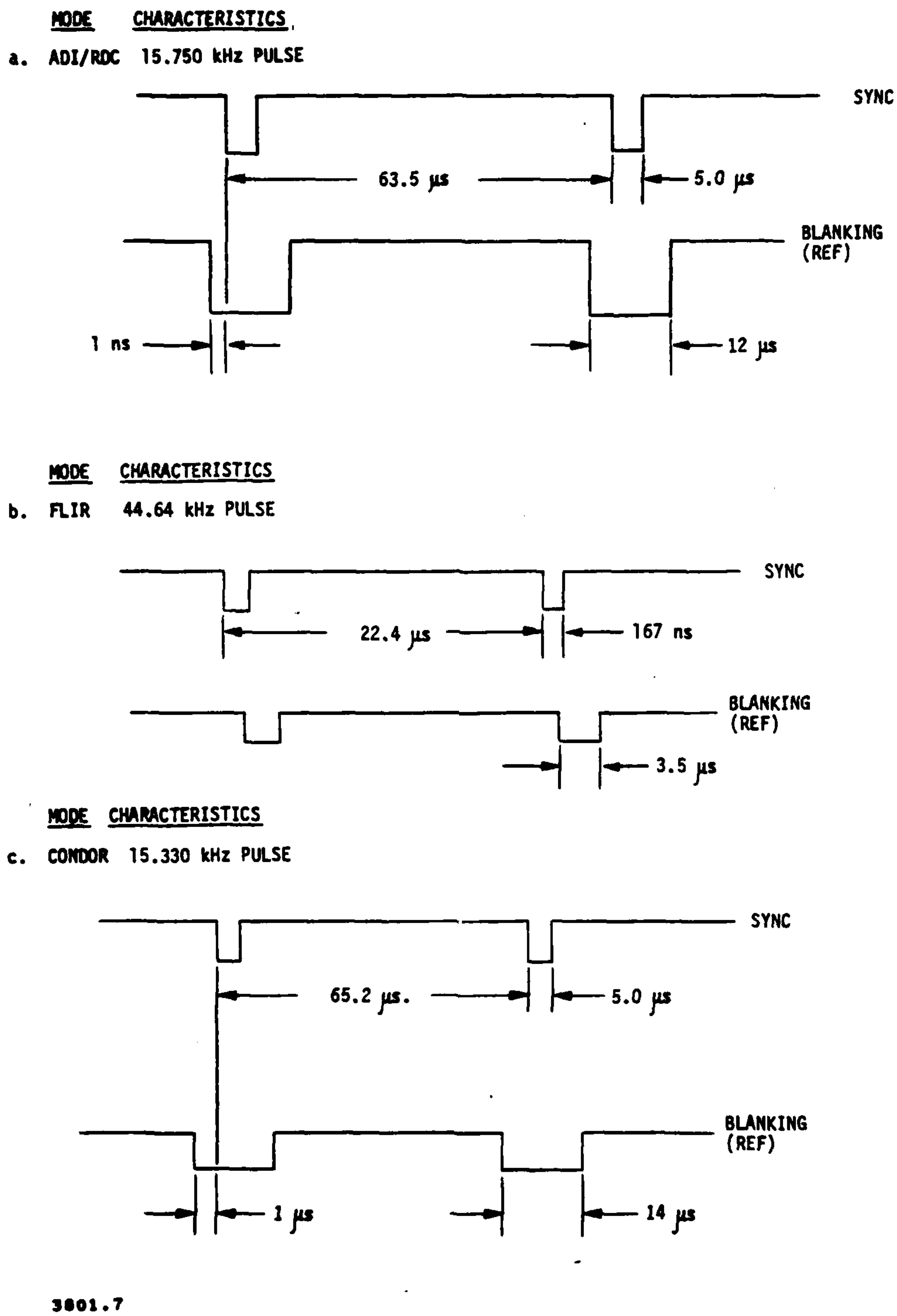


Figure 1-40. Sync Parameters

1.5.5.3 FIELD SWEEP DEFLECTION (SCHEMATIC 32221). The field sweep deflection (FSD) generates sawtooth sweep current at the field rate, 60 Hz. Linearity correction circuitry compensates the sweep sawtooth for CRT non-linearities, giving overall system linearity of $\pm 2\%$. Sweep requirements vary according to mode, as listed below:

Mode	Raster Size (In.)	Sweep Direction
ADI & RDC	8.33	Bottom to top
FLIR	7.6	Left to right
CONDOR	5.7	Top to bottom

Figure 1-41 shows the organization of the circuit.

Display mode control signals switch the pertinent reference voltages that control the sweep size in the sawtooth generator, a Miller integrator. These control signals also select the required sweep offset in the sawtooth generator.

An active reference circuit is incorporated in the sawtooth generator to compensate for varying component parameters.

The field deflection sawtooth voltage waveform is fed through a multiple breakpoint linearity correction circuit which modifies the slope of the sawtooth so that CRT non-linearities are compensated.

The linear deflection amplifier is a direct-coupled feedback amplifier which operates as a voltage-to-current converter. The amplifier converts the linearity-corrected field deflection sawtooth voltage waveform to an equivalent current drive waveform through the yoke load.

The deflection circuit is disabled if the sync input is absent.

An analog switch pulsing circuit has been designed in this assembly that utilizes the vertical sync pulse to excite all the analog switches in this assembly and the system at unit turn-on.

1.5.5.4 VIDEO AMPLIFIER (SCHEMATIC 32236). The video amplifier performs the following functions:

- Amplifies CONDOR, ADI/RDC, and FLIR video sufficiently to drive the cathode of the CRT. A linear relationship exists between voltage excursions of input signals and the corresponding luminance on the face of the CRT.

- Strips ADI/RDC and CONDOR line and field syncs from the composite video input. The line and field sync are used to synchronize the line and field deflections. The field sync is used to blank the CRT.

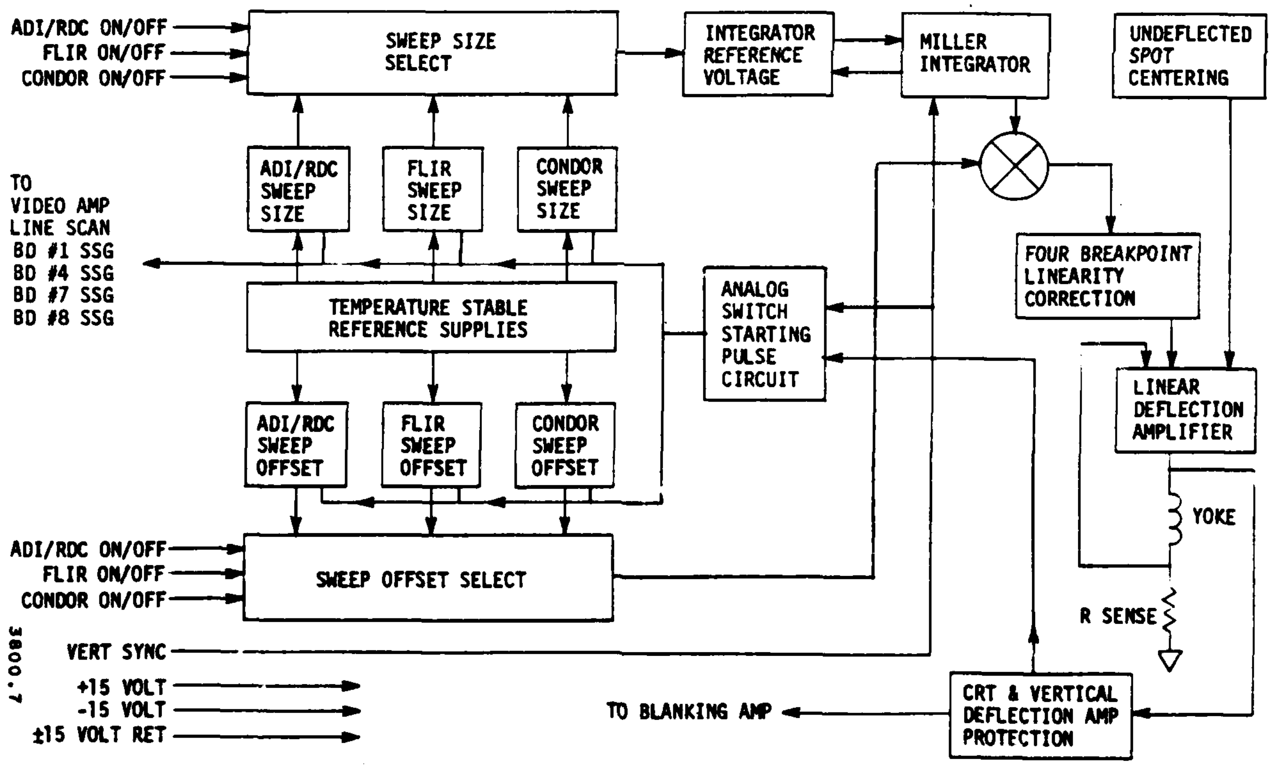


Figure 1-41. Field Sweep Deflection Block Diagram

- Strips FLIR field blanking to synchronize the field deflection and blank the CRT.

- Generates field blanking during ADI/RDC and CONDOR modes; this signal is synchronized with the corresponding field sync signal.

- Mixes the line blanking signal from line scan deflection with the field blanking signal to blank the CRT during sweep retrace.

- Blanks the CRT as a function of INS roll (input 44), INS pitch (input 45) and line scan and field scan failure signals.

- Provides CRT phosphor protection for system failure as discussed fully in paragraph 1.5.5.8.

Figure 1-42 shows the organization of the video amplifier.

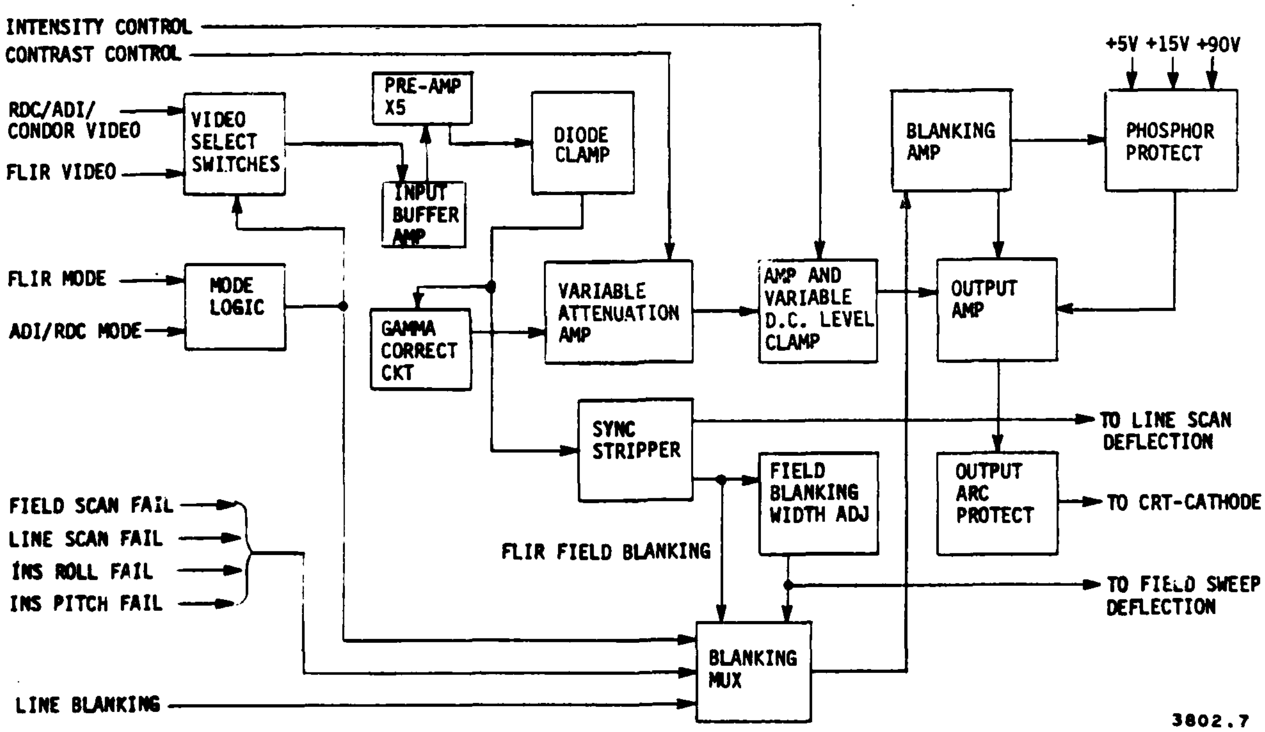


Figure 1-42. Video Amplifier Block Diagram

Video to be displayed is selected as a function of the mode control signal via mode logic and video select switches. The selected video is then terminated and buffered by the input buffer differential amplifier.

The video signal is amplified by approximately a factor of 5 at the preamp stage. Then the video is clamped at the sync level.

The video signal branches to the sync stripper and the gamma correction circuitry.

The gamma correction circuit corrects the video signal to cancel non-linearities associated with driving a CRT with a linear voltage.

The corrected video is operated on by an externally controlled variable attenuation amplifier which controls the contrast of the display. Then, the video is clamped and dc level controlled by the brightness control potentiometer which is externally controlled by the pilot. The video signal is then buffered and amplified by the output amplifier circuit. The output of the amplifier is clamped so that the cathode potential can never go below ground. CRT and amplifier protect circuitry protects the CRT phosphor from system failures by cutting the CRT off and protects the output amplifier from CRT arcing. Refer to paragraph 1.5.5.8.

The sync stripper separates field and line sync pulses from ADI/RDC and CONDOR composite video, and line and field blanking from FLIR video. The stripped line sync drives the line scan deflection. The stripped field sync goes from the stripper to a pulse shaper so as to sharpen the edges and fix the pulse width to 500 μs. The field drive or blanking pulse then goes to the field sweep deflection SRA and blanking multiplexer of the video amp SRA. A blanking multiplexer selects either the ADI/RDC, CONDOR, or FLIR field blanking pulse and sums it with the line blanking pulse from the line scan deflection. Also, four system failure signals are summed into a composite blanking pulse. The composite blanking pulse is channeled through an amplifier to the output stage of the video amp to blank the CRT such that blanking will override any video signal.

Table 1-8 summarizes input and output signal characteristics. Table 1-9 summarizes video amplifier characteristics.

1.5.5.5 ROLL SERVO & YOKE (SCHEMATIC 32311). The roll servo rotates the yoke in response to a roll angle command.

Figure 1-43 shows the functional organization of the roll servo, and table 1-10 summarizes the input/output parameters.

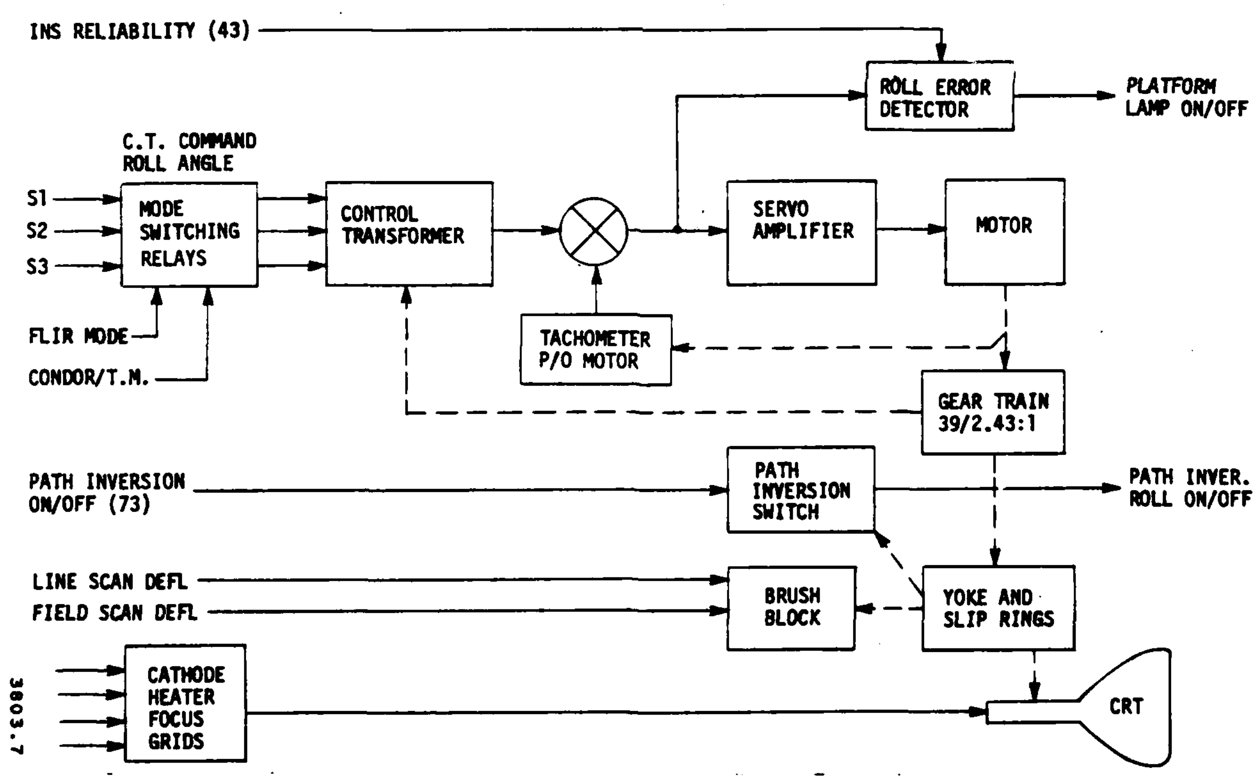


Figure 1-43. CRT/Yoke/Roll Servo Block Diagram

Table 1-8. Input/Output Signal Characteristics

Input	Output	Signal	Source	Z Load	Description
X		1. RDC/ADI composite	Symbol Generator	75Ω	Analog signal -0.4V = sync 0V = black 1V = white
X		2. FLIR composite video	DRS	75Ω	Analog signal -5V = blanking -3V = black +3V = white
X		3. CONDOR composite video	CONDOR	75Ω	Analog signal -0.4V = sync 0V = black +1.1V = white
X		4. FLIR mode	Symbol Generator	TTL output	+5V = FLIR mode 0V = off
X		5. Field sweep failure	Field Sweep Deflection	TTL logic	5V = fail 0V = good
X		6. Line scan failure	Line Scan Deflection	TTL logic	5V = fail 0V = good
X		7. INS roll fail	INS	2k (Min.)	0V/open = fail 28V = good
X		8. INS pitch fail	INS	2k (Min.)	0V/open = fail 28V = good
X		9. Contrast	Pilot's Control Panel	75k (Min.)	0V to +30V
X		10. Intensity	Pilot's Control Panel	100k (Min.)	0V to +15V
X		11. Line blanking	Line Scan Deflection	TTL logic	0V = blanking
X		12. ADI/RDC mode	Symbol Generator	TTL output	+5V = ADI/RDC mode 0V = off
	X	13. Video output	CRT Cathode	Capacitive 7 pF→10 pF	Negative - going video 60V = black 0V = max white +90 = blank
	X	14. ADI/RDC & CONDOR line sync	Line Scan Deflection	TTL logic level	5V = sync 0V = off
	X	15. Field blanking	Field sweep Deflection	TTL logic level	5V = sync 0V = off Pulse width ADI/RDC/CONDOR - 500 μs FLIR - 500 μs
	X	16. ADI/RDC & CONDOR line sync test	WRA Test	TTL logic level	0V = sync 5V = off Pulse width ADI/RDC & CONDOR = 5 μs FLIR = 3.5 μs

Table 1-8. Input/Output Signal Characteristics (Continued)

Input	Output	Signal	Source	Z Load	Description
	X	17. Field blanking test	WRA Test	TTL logic	0V = sync 5V = off Pulse width ADI/RDC & CONDOR = 500 μs FLIR = 500 μs
	X	18. Video amp output test	WRA Test	50k Min.	0V = white 9V = black
	X	19. HVPS enable	HVPS	10k Min.	5V = HVPS disable 0V = HVPS enable
	X	20. HVPS enable test	WRA Test	10k Min.	5V = HVPS disable 0V = HVPS enable

Table 1-9. Video Amplifier Characteristics

Blanking level:	70V nominal
Signal sense:	Drives cathode of CRT. Negative-going turns CRT on.
Cathode modulation:	60V p-p minimum
Rise and fall times:	Nominal 30 ns 10-90% at 60V p-p with capacity to ground of 8 pF
Bandwidth:	16 Hz to 12 MHz minimum
Gamma correction:	Linear light output $\pm$ 20%
Output arc protection:	Amplifier protected from damage caused by CRT arcing.
Phosphor protection:	In the event of system failures, the output of the video amplifier cuts the CRT off. HVPS disabled when the 90V power supply drops 25%, as sensed by circuitry in the video amplifier.

Table 1-10. Roll Servo Inputs and Outputs

Input	Input No.	Source	Description
Roll Command S1	37	INS	From Kearfott Stator
Roll Command S2	38	INS	PN R1001-1A
Roll Command S3	39	INS	PN R1001-1A
INS Reliability	43	INS	PN R1001-1A
Path Inversion on/off	73	Ballistic Computer	0/28V D.C.
Line Scan Deflection Waveform	N.A.	LSDC	0/28V D.C.
Field Scan Deflection Waveform	N.A.	FSD	
Video	N.A.	Video Amplifier	40 Hz - 12 MHz 50V p-p
Blanking	N.A.	Video Amplifier	60V p-p
FLIR mode on/off	N.A.	Sym. Gen.	0V = OFF 5V = ON
CONDOR/T.M. on/off	N.A.	Sym. Gen.	0V = OFF 5V = ON

Output	Destination
Path Inversion/Roll on/off	Symbol Gen.
Platform Reliability	Platform Reliability Lamp

The servo/yoke assembly is capable of rotating at 360 degrees/second (60 rpm) with a typical 12 in-oz friction load, and is capable of of 0.2 degree resolution.

With a step input, the assembly rotates at 360 degrees/second with a typical yoke assembly inertia of 0.5 oz. in. second^2 and 12 in-oz friction load.

The path inversion switch is closed at $\pm$110 $\pm$10 degrees roll angle.

1.5.5.6 LVPS (SCHEMATIC 32141). The LVPS generates all voltages required for operation of the XJ-1, except the high voltages for the CRT.

Figure 1-44 shows the functional organization of the LVPS.

Start-up power for the internal supply is provided by a single-phase 400 Hz transformer. This power is overridden by an output from the DC-to-DC converter to improve efficiency. The internal supply provides power to operate the oscillator, the switching regulator, the feedback regulator and the overvoltage and overcurrent circuitry. It also provides 115 Vac and 11.6 Vac to the synchro and 6.3 Vac for the CRT filament.

The oscillator provides complementary squarewave drive signals at 15.75 kHz for the DC-to-DC converter, and 31.5 kHz squarewave drive signals for the switching regulator.

The 3-phase input power for the DC-to-DC converter is rectified and filtered to 268 Vdc and then switch mode regulated.

The switching regulator converts the 268 volt dc input to 130 volts dc by controlling the duty cycle of a power switch, minimizing power dissipation in the regulator itself. Feedback from the 5-volt output of the DC-to-DC converter varies the duty cycle of the switch to increase or decrease power to the DC-to-DC converter as required by the load.

The DC-to-DC converter uses the squarewave signals from the oscillator to switch the 130 volt input at the transformer primary. The outputs of the transformer are rectified and filtered for the Zener regulators, the series regulators and the 5-volt output. The 23-volt output is provided for direct use by the indicator unit with no further regulation.

The feedback circuit compares the 5-volt output with an internal reference and pulse-width modulates the switching regulator through the coupling transformer in the switching regulator base drive. Modulation controls the amount of power required by the DC-to-DC converter to produce a constant 5 volts.

The overvoltage circuit uses a level detector to remove the internal base drive from the switching regulator. It also triggers an SCR across the 5-volt output to limit excessive voltages from being applied to the load.

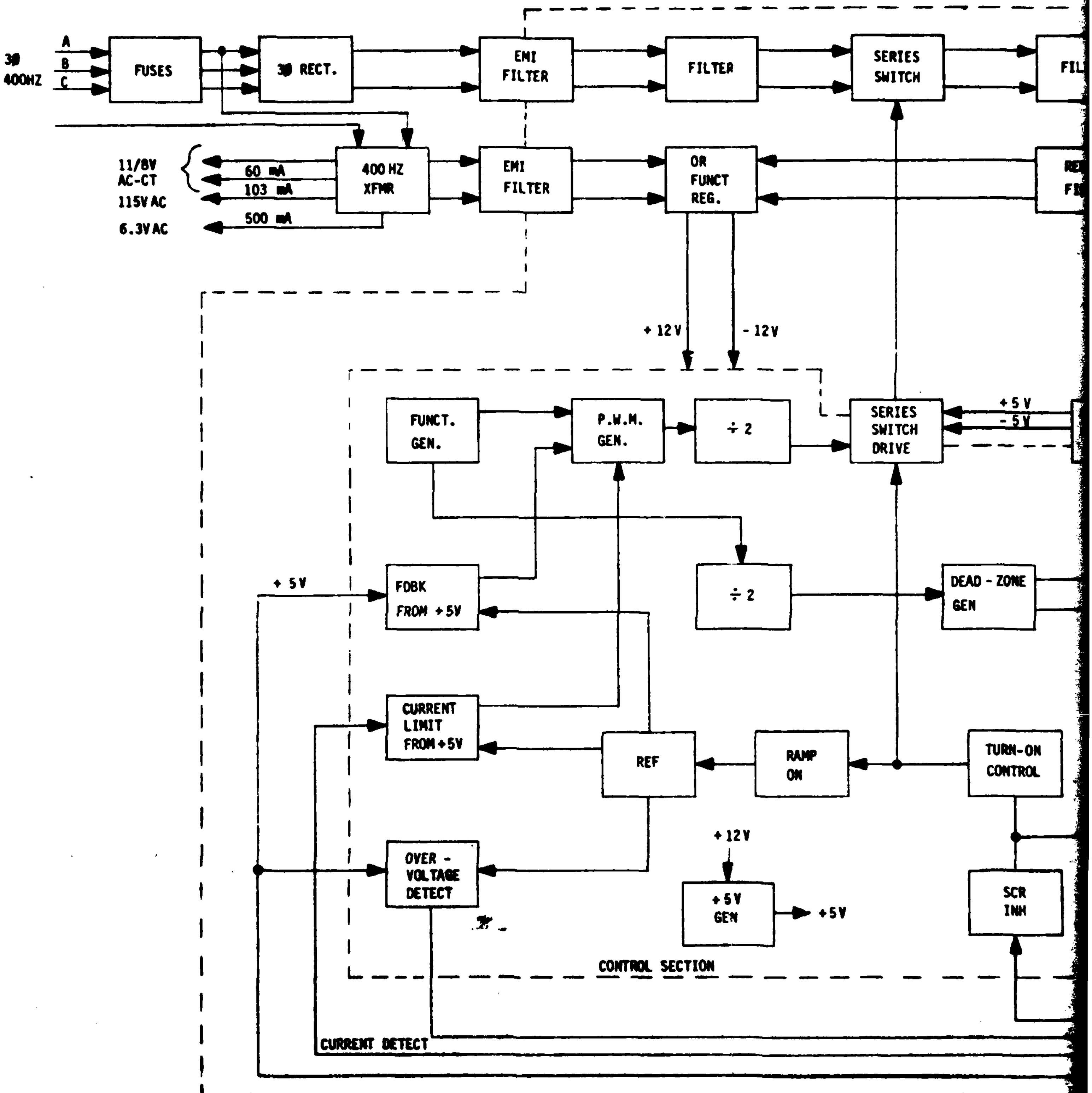
The ±15 and +10-volt regulators are linear series regulators using the filtered outputs from the DC-to-DC converter. The regulators are integrated circuits with external power handling, filtering, and protection components. They use feedback from the outputs to control the voltage and are protected from short-circuits by current-limiting circuitry around the integrated circuits. Overvoltage circuitry is also incorporated into the regulators to actuate the current limit and shut down the regulator.

The ±30 and +90-volt regulators are Zener regulators using the filtered outputs from the DC-to-DC converter. The regulators are protected from short-circuits by series resistors limiting current until rectifier diodes open. Overvoltage protection is provided by the Zener itself.

Rectified unregulated voltages of +15, +28, and +34 volts are supplied also for deflection circuitry, roll servo, and HVPS.

The input of the LVPS is 115 Vac, 400 Hz, 3-phase, 4-wire WYE. Steady-state voltage limits are as defined in MIL-STD-704A, Table I for Category B Emergency Power; these limits are applicable during 380-420 Hz operation. The LVPS will not be damaged by an steady-state design limit excursions defined in MIL-STD-704A. The LVPS will continue to operate with a loss of one phase with only an increase in p-p ripple on the digital +5 V line.

The LVPS provides the voltages for the respective load conditions specified in table 1-11.



3Ø
400HZ
A
B
C
FUSES
3Ø RECT.
EMI FILTER
FILTER
SERIES SWITCH
11/8V AC-CT
115V AC
6.3V AC
60 mA
103 mA
500 mA
400 HZ XFMR
EMI FILTER
OR FUNCT REG.
+ 12 V
- 12 V
FUNCT. GEN.
P.W.M. GEN.
÷ 2
SERIES SWITCH DRIVE
+ 5 V
- 5 V
+ 5 V
FDBK FROM + 5V
÷ 2
DEAD - ZONE GEN
CURRENT LIMIT FROM + 5V
REF
RAMP ON
TURN-ON CONTROL
+ 12 V
OVER - VOLTAGE DETECT
+ 5 V GEN
+ 5 V
SCR INH
CONTROL SECTION
CURRENT DETECT

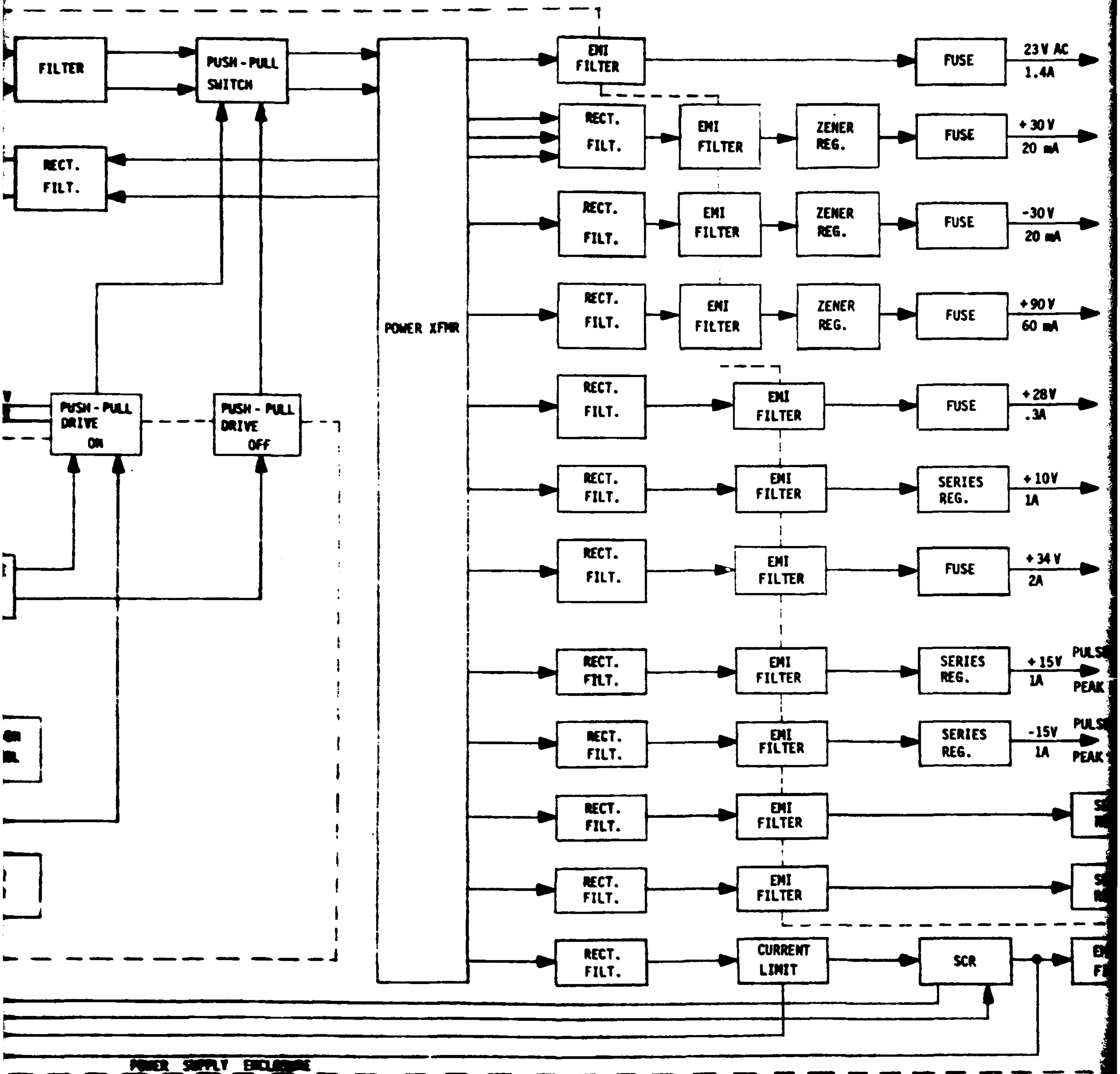
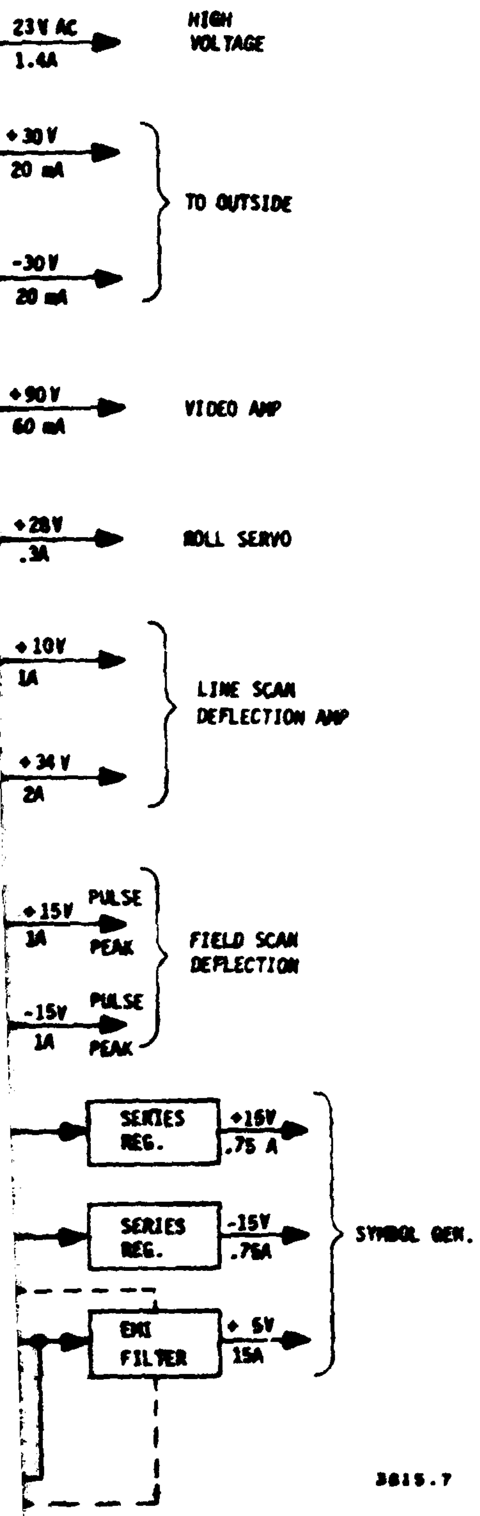

FILTER
PUSH - PULL SWITCH
RECT. FILT.
POWER XFMR
PUSH - PULL DRIVE ON
PUSH - PULL DRIVE OFF
EMI FILTER
FUSE
23 V AC
1.4A
ZENER REG.
+ 30 V
20 mA
-30 V
20 mA
+ 90 V
60 mA
+ 28V
.3A
SERIES REG.
+ 10V
1A
+ 34 V
2A
+ 15V
1A
-15V
1A
CURRENT LIMIT
SCR
POWER SUPPLY ENCLOSURE

Figure 1



gure 1-44. LVPS Block Diagram

Table 1-11. LVPS Outputs

OUTPUT VOLTAGE (V)	TYPE OF REGULATION (NOTE 1)	REGULATION				NOMINAL LOAD CURRENT (A)	MAXIMUM LOAD	
		LINE	LOAD	TEMP	WORST CASE		CURRENT (A)	POWER (W)
+90	Z	1%	5%	4%	±10%	0.03	0.06	5.4
+30	Z	--	--	--	--	--	0.02	0.6
-30	Z	--	--	--	--	--	0.02	0.6
+34	U	1%	5%	4%	±10%	1.1	2.2	74.8
+28	U	1%	5%	4%	±10%	0.2	0.3	0.8
+23	U	1%	5%	4%	±10%	1.1	1.4	32.2
+15	R	.1%	.4%	.5%	1%	1.1	1.5	22.5
+15	R	.1%	.4%	.5%	1%	1.1	1.5	22.5
-15	R	.1%	.4%	.5%	1%	1.1	1.5	22.5
-15	R	.1%	.4%	.5%	1%	1.1	1.5	22.5
+10	R	.1%	.4%	.5%	1%	1.4	2.0	20.0
+5.0	D	.2%	.8%	1%	±2%	11.0	14.0	70.0
115 ac	NONE	--	2%	--	±2%	0.2	0.20	23.0
11.6 ac	NONE	--	2%	--	±2%	0.03	0.05	0.6
6.3 ac	NONE	--	2%	--	±2%	0.60	1.0	6.0

NOTE: 1. Z - Zener, U - Unregulated, R - Regulated, D- Digital Supply

1.5.5.7 HVPS (SCHEMATIC 32321). The HVPS supplies the CRT second anode and G2 voltages. Input power is nominal +24V unregulated, with a tolerance of +5, -2V. Outputs are as listed below:

Output	Parameters
15 kV nominal adjustable from 14.5 kV to 15.5 kV	Current, 750 μA Ripple, 5V p-p maximum Regulation 0.4% @ 100 μA
500V nominal, range from 475 to 525V	Current, 50 μA Ripple, 2V p-p maximum Unregulated

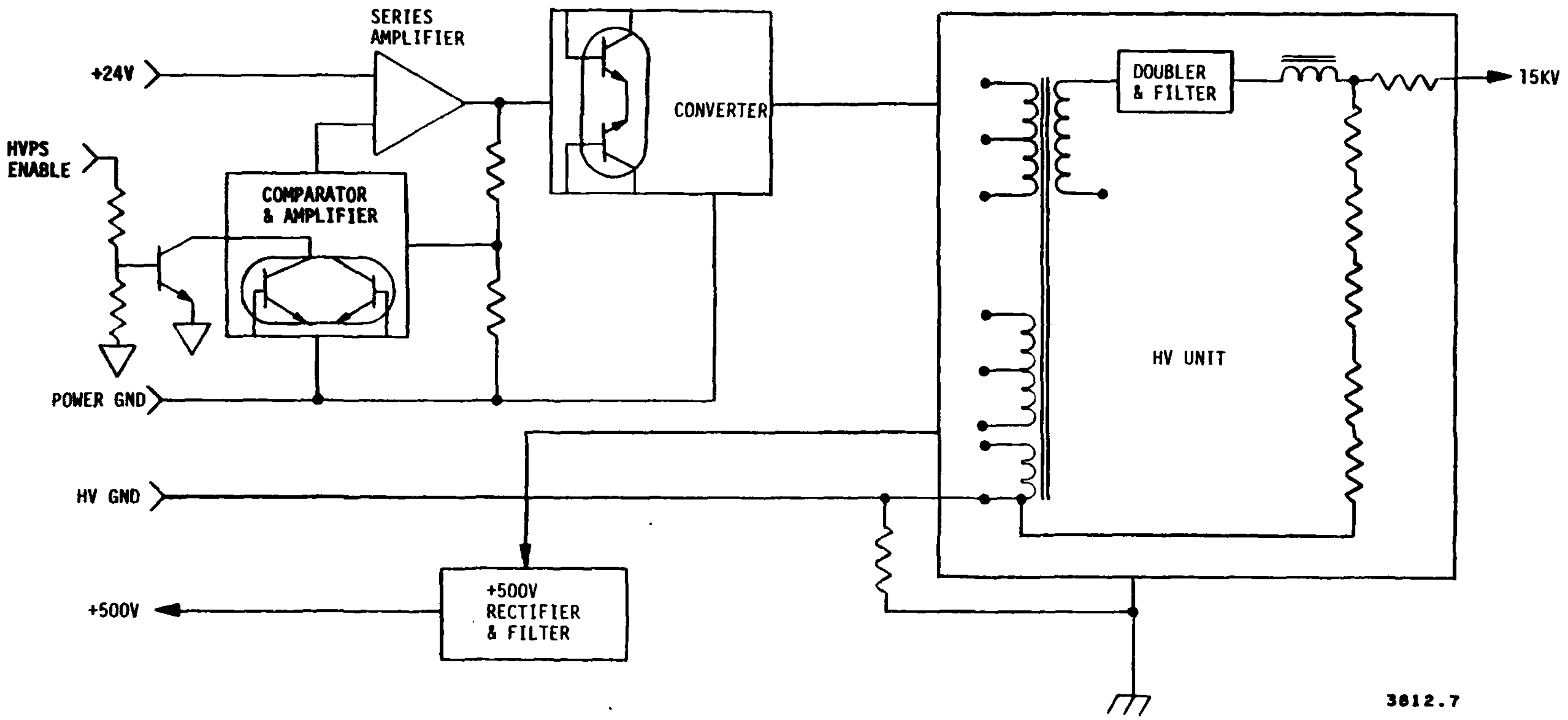


Figure 1-45. HVPS Block Diagram

1.5.5.8 PHOSPHOR PROTECTION. Phosphor burn of the CRT is potentially the major cause of CRT failure. Protection circuitry has been incorporated into the XJ-1 to prevent phosphor burn on the CRT due to the following system failures:

A) Loss of line scan deflection
B) Loss of field scan deflection
C) Simultaneous loss of both line scan and field scan deflections
D) Removal of deflection SRA
E) Loss of any power supply or combination of power supplies

The following paragraphs analyze the above failure mechanisms, and explain what protection is provided in the XJ-1 to prevent phosphor burning.

Loss of either the line scan and/or field scan deflection (conditions A through D) limits the travel of the electron beam, thereby heating up the CRT phosphor. Sweep rate detection circuitry, incorporated on both the line scan and field scan SRA's, detects the loss of sweep drive voltage; pertinent parts of the schematic diagrams are shown in figure 1-46.

For the field scan SRA, the circuit analysis proceeds as follows. Sweep drive voltage to the CRT field yoke winding is ac coupled through a sense resistor (not shown) and capacitor A to an integrator composed of amplifier B, diode,C, capacitor D, and resistor E. Decay time of the integrater has been calculated such that the integrator voltage is below the threshold set by resistors F and G within 8 frame periods.

$$\text{Threshold} = \frac{R_G}{R_G + R_F} \times 15V = \frac{560}{15560} \times 15V \approx 0.54V$$

Since the capacitor charges to 15V - 0.62V = 14.38V (diode drop), the required integrator decay is

$$\frac{0.54V}{14.38V} = 0.038V$$

The number of time constants required is:

$$-\ell n\ 0.038 = 3.282$$

In seconds, this corresponds to:

$$\text{Decay time} = 3.282 \times 33000 \times 2.2 \times 10^{-6} \text{ farads}$$

$$= 0.238 \text{ seconds}$$

One frame of 525-line video is 0.033 seconds, therefore, the number of frames required to exceed the threshold is:

$$\frac{0.238 \text{ seconds}}{0.033 \text{ seconds}} = 7.2 \text{ frames}$$

Output of amplifier H is then clamped by resistor I and diode J, and used to drive the sweep fail logic on the video amplifier.

Analysis of the sweep failure circuit on the line scan deflection proceeds in a manner similar to the above. In this case, the time constants are adjusted to provide a delay of 5 FLIR horizontal lines, or approximately 110 microseconds.

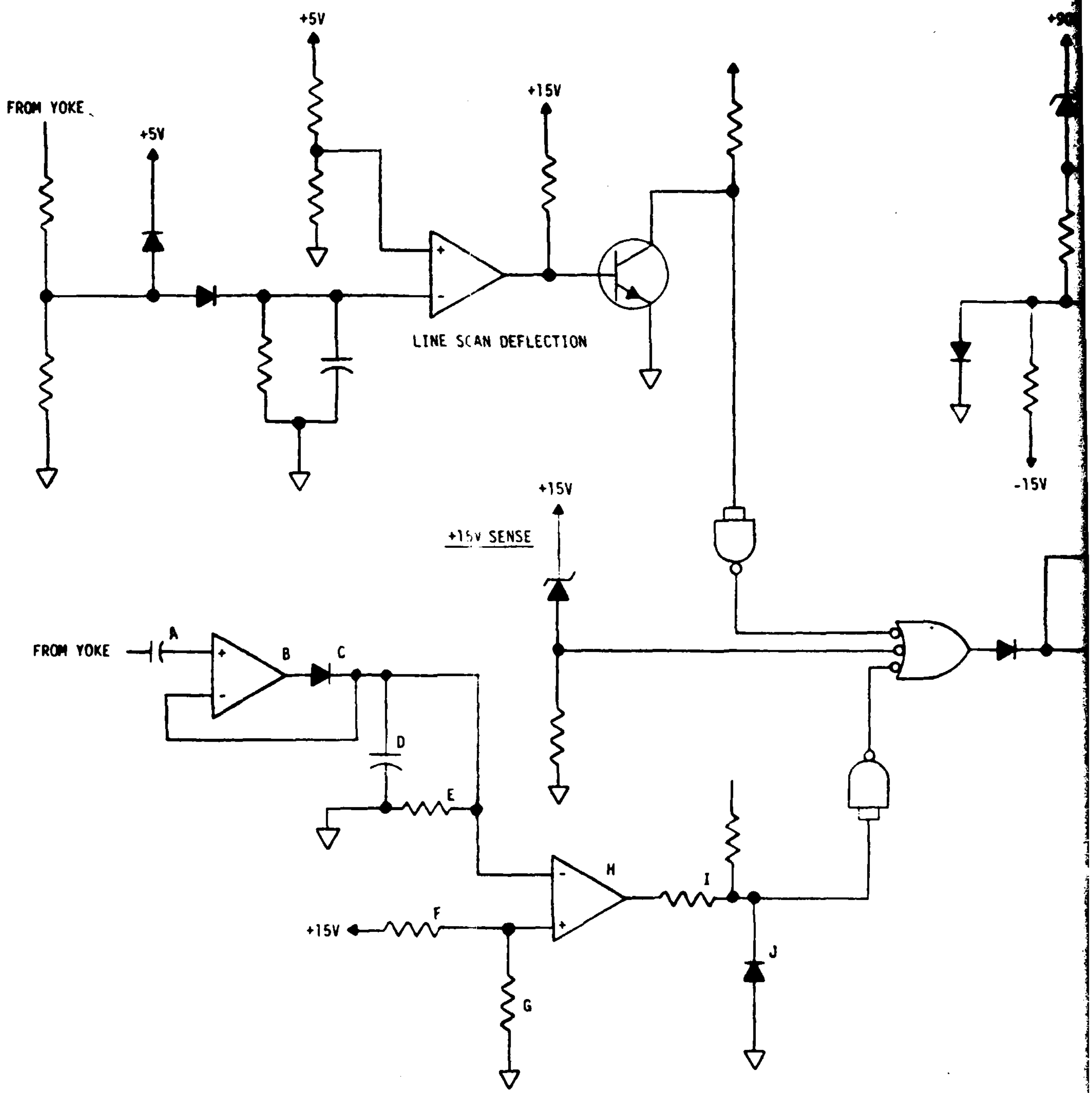
Both the line scan and field scan sweep failure circuitry is organized such that a current sink is required to indicate a GO condition; an open circuit or a high level implies a sweep failure. This logic polarity provides a NO-GO signal whenever the field scan and/or line scan is removed from the circuit, eliminating CRT burning due to condition D - Removal of deflection SRA.

Condition E - Failure of Power Supplies can adversely affect the CRT in two ways. First, the loss of the 90V prevents the video amplifier from blanking the CRT, since the cathode cannot be driven to cut off. The second condition is the failure of the sweep protection circuitry due to loss of its energizing voltage.

The XJ-1 senses an out-of-tolerance condition in the +90V supply and shuts down the HVPS. This sense circuitry also blanks the output video stage using the diode-decoupled +90 Vdc to hold the CRT cutoff until the HV decays to a safe voltage.

A second sense circuit blanks the CRT if the +5 Vdc power supply voltage falls below +3.5 Vdc.

A third circuit senses when the +15V supply drops below +14V. When the above occurs the blanking amp cuts off the CRT.



LINE SCAN
DEFLECTION

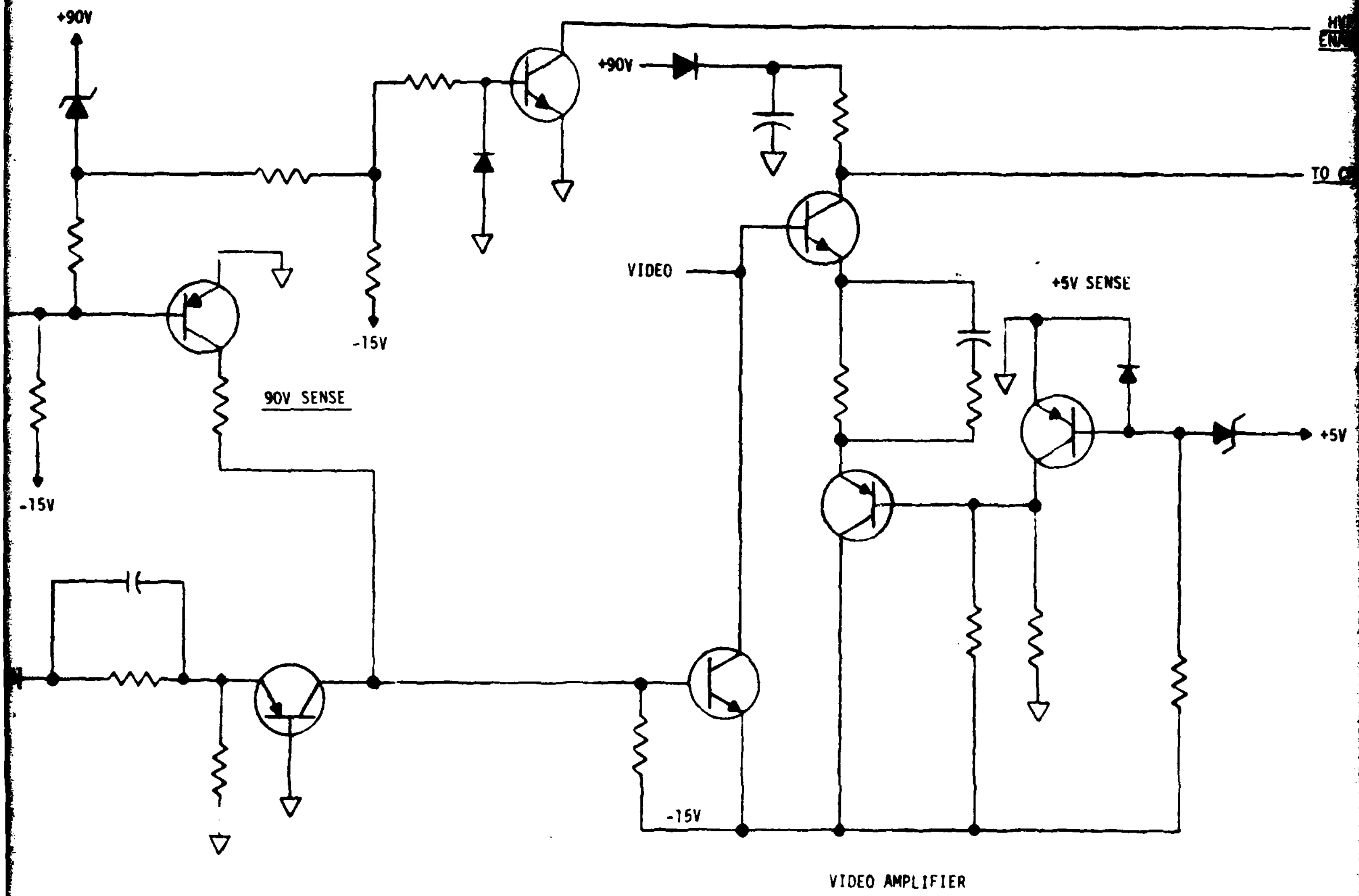


Figure 1-46. CRT Protection Cir

2

HVPS ENABLE

TO CRT CATHODE

+5V

13.7

ion Circuitry

3

1.5.6 Test Set. The primary test equipment for the XJ-1 display consists of the old ADI test set 1956-49 and the XJ-1 adapter box (figure 1-5). At one time this adapter box was identified as the TRAM adapter test set. The XJ-1 adapter box not only supplies TRAM video modes but also inputs for the new symbology utilized in the XJ-1 display format.

The old ADI test set supplies the necessary discrete on/off voltages and analog inputs for positional data of the symbols. This test set has the capability for selection of the contact analog, terrain clearance, and test modes. This test set routes primary power to the unit. This test set provides controls for the following symbols:

- Flight path
- Weapon symbol
- Flight path border
- Flight path center line
- Command heading lines
- Impact/stall symbol
- Target symbol, offset impact point
- Pitch trim cursors
- Roll Pointer
- Pitch lines
- Ground texture
- Pull-up marker
- Release marker
- Offset impact point

This test set provides control to illuminate the indicator lights on the annunciator panels.

The XJ-1 adapter test set is connected as shown in figure 1-47. The adapter provides shades of gray, resolution bursts, and cross hatch video for the TRAM modes, consisting of FLIR mode and CONDOR/external mode. The FLIR mode has a 44 kHz line rate and 60 Hz field rate video (fixed amplitude format); separate sync outputs are provided for both TRAM modes. The CONDOR/external video mode has a 15.33 kHz line rate and a 60 Hz field rate video format.

This test set provides synchro outputs for the magnetic/true heading symbology, as well as analog voltages, discrete (on/off signals), and control for radar altitude, angle of attack, ILS/ACLS cross pointer symbology, and vertical speed indicator.

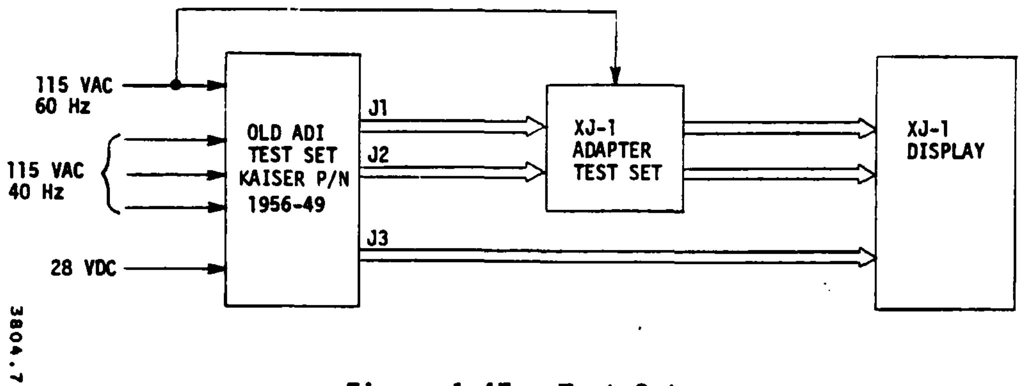


Figure 1-47. Test Setup

1.6 GENERAL DATA

The following documents are applicable to the XJ-1 and are listed for reference:

Kaiser

32591	VDI Design Requirements
32004	Installation Drawing
32016	Configuration Control
32361	Thermal Design
32066	Acceptance Test Procedure
13022	Qualification Test Procedure
13027	Reliability Demonstration Test Procedure
13032	Flight Worthiness Test Report
13199	Qualification Test Report
ETR-77-03	Reliability Demonstration Test Report
ETR-76-04	A6 HRD Failure Rate Predictions

NAVAIR

NAVAIR 01-85ADA-2-7.3	Intermediate Maintenance Manual for Analog Display Indicator IP-722( )/AVA-1*

*Presently deployed, predecessor of XJ-1.

1.7 DETAIL DATA

1.7.1 General

The following paragraphs present an overview and detailed discussion of the design, integration, and testing activity on the XJ-1.

1.7.2 Design Activity

Design activity began in November 1974 and was essentially finished by September 1975, with sustaining activity continuing as required. A preliminary design review was held at the Kaiser facility on February 1975, and a critical design review on May 20, 1975.

1.7.3 Integration

Functional integration of the XJ-1 subassemblies began on or about November 1975 at the Kaiser facility, and concluded in February 1976. System integration with the aircraft avionics began in May 1976 at the Navy Air Test Center facility, and concluded in March 1977, with sustaining effort as required.

1.7.4 Flight Test

1.7.4.1 GENERAL. An evaluation of the redesigned IP-722 (XJ-1) AVA-1 Analog Display Indicator (ADI) was conducted to determine the suitability of the display for the all-weather attack mission of the A-6E Target Recognition Attack Multisensor (TRAM) airplane and to identify enhancing characteristics and/or deficiencies to permit timely correction prior to production. Both ground and flight tests were conducted. Twenty-eight flights were flown for a total of 43.2 flight hours. Four characteristics, including presentation of essential flight information and high quality forward-looking infrared imagery on the ADI, enhanced the capability of the A-6E airplane to carry out the all-weather attack mission. Eight Class I deficiencies should be corrected prior to production, including ADI power dropout when the right generator drops off the line. Thirteen Class II deficiencies should be corrected as soon as practicable. One Class III deficiency should be avoided in the next design phase. The redesigned IP-722 (XJ-1) AVA-1 ADI demonstrated excellent potential to provide all essential flight and attack information for the all-weather mission of the A-6E TRAM airplane.

Lt. Marty Gunther was the flight test pilot who coordinated the test program. For many of the flights, movies of the display were taken. Consequently, Lt. Gunther has collected substantial film footage of the FLIR presentation and various contact analog modes during flight. Table 1-12 lists the Class I, II and III deficiencies which were identified by Lt. Gunther at this stage of testing. Other flight testing was accomplished by the Navy's Operational Evaluation Group at China Lake, CA. (VX-5).

In general, pilots who have been exposed to the XJ-1 like it and want this new display in the fleet. Below is a list of pilots and B/N's who have flown with or been demonstrated the XJ-1.

Pilots	B/N's
Commander Don Boecker	Lt. Todd Cleland
Lt. Commander Dave Newton	Lt. Dave Anderson
Major Bob Newsom	Lt. Bud Jewitt
Lt. Dave Strong	

Table 1-12. Class I and II Deficiencies Noted During Flight Test

ITEM	DEFICIENCY	CLASS	SOLUTION	DESCRIPTION*
1.	Problem with fuse holder	I	Change fuse holder.	Phase A. Four fuses changed. Phase B. Modify LVPS casting to change the five fuse holders. Redesign casting tooling.
2.	HRD power drop-out occurs when aircraft generators are switched	I	Redesign LVPS to avoid drop-out.	Phase B - Relayout board A-4 in LVPS.
3.	Poor FLIR video presentation	I	Design a FLIR MOD to accept existing FLIR video.	Redesign interface and add AGC. Requires modifying FLIR video input buffer and scaling circuitry on video amplifier. Phase B - Relayout video amplifier board.
4.	-10^{0} FLIR cutout angle unacceptable	I	Change G.A.C. software to reduce cutout angle. No action required by KE.	N.A.
5.	Vertigo induced when switching from FLIR to contact analog modes	I	Design a circuit to blank the display during mode switching.	Add new circuit to Roll Servo PWB to blank display during all mode switching. Phase B - Relayout Roll Servo PWB.

Table 1-12. Class I and II Deficiencies Noted During Flight Test (Continued)

ITEM	DEFICIENCY	CLASS	SOLUTION	DESCRIPTION*
6.	Poor RDC range bin contrast	I	Redesign RDC video mixer.	Add new circuit to T.C. input board 6 to compensate for gamma correction in video amplifier. Phase B - Relayout board 6.
7.	Pathway obscures symbology in TC mode	I	Design a circuit to set pathway brightness to zero in TC mode.	Add gating circuit to path to inhibit in TC mode. Phase B - Hardware change, or incorporate as part of Item 6.
8.	Handle too short to carry XJ-1 when inclinometer is attached	I	Increase handle length ½" and add retaining clips to sides of handle	Move connector inside Bezel, machine hand grip, relocate retaining clips.
9.	Problem with night filter stowage	II	Redesign filter stowage mech. (Assumes use of double-notch filter.	Redesign night filter levers to improve operation. Phase B - Update tooling.
10.	Double-notched band-pass day filter results in washed-out display	II	Redesign for single-notch day filter (2-filter config.)	Modify bezel and day filter such that day and night filters are installed separately. Phase B - Update drawings and modify bezel casting tooling.

Table 1-12. Class I and II Deficiencies Noted During Flight Test (Continued)

ITEM	DEFICIENCY	CLASS	SOLUTION	DESCRIPTION*
11.	Radar ALT/VSI scales are not visible on range bins in TC mode	II	See Item 6.	Add new circuitry to board 3 to provide blanking box for scale. Modify video mixer, board 6. Phase B - Relayout board 3.
12.	Attitude overshoot when passing through $+90^{0}$ pitch	II	Gain problem. No KE action required.	N.A.
13.	Loss of A/C attitude symbology in FLIR mode	III	Incorporate TDTA for FLIR cutout. No KE action required.	Major design modification. May not fit in box.
14.	Vertical speed symbol is oversensitive	II	Increase VSI damping.	Modify VSI input filter on board 1. Phase B - Relayout board 1.
15.	Inadequate zero reference for VSI symbol	II	Highlight zero index of VSI with a black border.	Modify VSI circuitry on board 5 and video mixer. Phase B - Relayout board 5.
16.	AOA symbol oversensitive	II	Increase AOA damping.	Modify AOA input filter on board 1. Phase B - Same as Item 14 above.
17.	AOA symbol is too coarse	II	Redesign AOA symbol.	Modify AOA circuitry. Phase B - Same as Item 15 above.

Table 1-12. Class I and II Deficiencies Noted During Flight Test (Continued)

ITEM	DEFICIENCY	CLASS	SOLUTION	DESCRIPTION*
18.	Brightness must be readjusted when switching between FLIR and contact analog modes	II	Design a FLIR AGC circuit.	Add new AGC board to system to compensate for FLIR input video amplitude changes. Phase B - Layout new board and mother board.
19.	Brightness control range unusable	II	Increase range of brightness control.	Brightness control of both display and pathway: usable limit is reached when controls are adjusted to approximately 50% cw.
20.	Distorted lettering annunciator lights	II	Correct in production.	Correct procedures in etching letters on annunciators.
21.	Abnormal peaking of pathway apex when level	II	G.A.C. software change. No action required by KE.	Investigate software fix by setting pathway curvature to zero until required or by storing the pull-up marker approximately ½" above the electronic center of display.
22.	Blanking of ground texture by pathway	II	See Item 7.	Modify video mixing circuitry on board 6 to allow trapezoids to be seen at all times. Phase B - Relayout board 6.

*Phase A - Modify SN 001. No formal documentation.
Phase B - Design and document for production.

Pilots

Lt. Marty Gunther

Lt. Craig Steidle

Lt. Ken Pyle

Lt. Dan Moore

The following paragraphs present details of the various activities that were performed during flight test.

1.7.4.2 EMI GROUND TESTS. The EMI ground tests were successfully completed at Patuxent River in the period 13-17 December 1976.

1.7.4.3 FLIR GROUND TESTS. The FLIR ground test results illustrate that the XJ-1 FLIR presentation is at minimum as resolvable as the Hughes FLIR display. In some cases the test operators compiled better data with Kaiser's FLIR presentation. Although the FLIR presentation is excellent when setup correctly, inherent FLIR interface problems still exist. There is an increase in display brightness in the FLIR mode and with high-amplitude video signals, black images on the display smear and an occasional loss of field deflection sync occurs. The problem will be resolved when the identification of the correct video amplitudes can be made by Hughes Aircraft.

1.7.4.4 VSI AND AOA DAMPING. After the first few evaluation flights Lt. Gunther requested modifications to the system. The damping of VSI and AOA symbology was increased by the addition of capacitors on the interface board.

1.7.4.5 BRIGHTNESS CONTROL. The brightness control range for the display and the flite path were reduced such that neither the display nor the path could saturate white. The brightness control modifications were accomplished by changing a resistor on the video amp and a resistor on board six.

1.7.4.6 MODE SWITCHING. When the pilot switches from FLIR to the contact analog mode the CRT yoke is rotated 90 degrees. During MODE transition the pilot views a display that momentarily presents incorrect attitude data; this presentation can induce vertigo. Kaiser extended the blanking time associated with changing into and out of FLIR mode to approximately 400 ms; this is approximately the amount of time it takes the yoke to roll 120°; 120° is the maximum initial roll that the yoke will experience when the computer-controlled FLIR cutout creates a mode transition.

The Navy pilots indicated that they prefer the display blanked during mode transitions and believe that a blank CRT during mode transitions is less likely to induce vertigo. The blanking time was extended by changing two resistors on the line scan subassembly. This solution will be insufficient since blanking will occur only for FLIR mode transitions and not for the other external video mode. A design fix for mode transition blanking will be incorporated during the production transition. Blanking will be a function of roll transition time.

1.7.4.7 As a result of the flight evaluation, the zero reference tick will be highlighted on the VSI scale. A highlighted tick mark will enable the pilot to quickly locate OFT/min. This can be accomplished with some circuit redesign and ROM reprogramming.

1.7.4.8 BLANKING FAILURE. A failure was experienced with the display at Pax River. A transistor failed in the blanking circuit on the video amplifier (Q14, JTX2N2369A). The part was substituted with an available JTX 2N2222A, a slower transistor. The result of this substitution caused a blanking band across the top of the display in FLIR mode. The failed component was given to Kaiser reliability for failure analysis. No system failure mode could be attributable to the failure of this part. A new transistor (JTX2N2369A) was installed into the video amplifier in April 1977 and no such failure has since occurred.

1.7.4.9 POWER DROP-OUT. Kaiser has investigated the power drop-out that was noted during flight test (see Item 2 of table 1-12). This item states that the display shuts off when the primary aircraft power generator is switched to the emergency generator. At this time, a transient of unknown magnitude occurs temporarily, triggering an input protection circuit that shuts down the system. It is then necessary to recycle power to get the display back on. This is an unacceptable condition, in situations such as during catapult launch.

The phenomenon was traced to the over-voltage protection circuit designed in the low voltage power supply. During generator power switching, a transient of an undefined nature causes the LVPS to crowbar into the protection mode and shut the display off. The protection circuit is designed to protect the five-volt logic devices from over-voltage when the LVPS senses a transient over/under input voltage condition.

Kaiser has designed and implemented into the flight test unit a voltage sensing circuit. This circuit still senses an out-of-tolerance input voltage transient condition and protects the XJ-1 by shutting it off; however, the voltage level is now sampled and sensed every 50 milliseconds. If an out-of-tolerance condition exists the system still shuts down, but if the input voltage returns to the specified limits the LVPS is recycled automatically to a normal operating condition within one second.

1.7.4.10 FLIR AGC. The FLIR presentation varies when the BN varies the gain control on the DRS FLIR display. A quick fix was incorporated into the flight test unit that enabled the pilot to view the FLIR display. Kaiser will have to design an automatic gain control circuit to accept this varying video and present an optimum FLIR display to the pilot.

1.7.4.11 DAY/NIGHT FILTER. The XJ-1 can provide the pilot with a crisp, clear and bright display. In a bright ambient light situation the optimum light filter to use with the system CRT (P43 phosphor) is a 15% single notch green bandpass filter. However (in the present configuration), this filter cannot be used in a red cockpit because a red night filter is attached over the green. The day bandpass filter absorbs all the visible wavelengths that are present in sunlight except for a very narrow band in the green spectrum that matches the CRT phosphor output. The result is that the red light emitted by the P-43 phosphor is absorbed by the green day filter. When the red night filter, which absorbs green light, is placed over the green day filter, the amount of visible light from the display that reaches the pilot's eye is unacceptable.

The old ADI used a CRT with P20 phosphor and a low-resolution, narrow-viewing-cone micromesh filter. This combination yields a marginal display as viewed by the pilot in daylight conditions; however, it is viewable at night when using a red filter.

As a result from the above, Kaiser attained from Medivac a "double-notch" filter for the flight test. The filter has a wider bandpass than expected. Both single-notched and double-notched filters have been utilized in flight. Pilot feedback on the two filters has been conflicting. Generally, the double-notched filter is not adequate for daytime use because it does not prevent the display from washing out. The single-notched filter has caused brightness problems when the pilot has his visor down. It is apparent that the Navy will require removable day and night filters if double-notched day filter technology cannot be attained. The double-notch filter technology is advancing sufficiently tc warrant optimism in a technological breakthrough before the initiation of production.

If new bandpass light filter technology cannot be attained, Kaiser proposes that each filter be removable so that optimum viewability may be obtained for both day and night conditions. The change to the system will require modifying the front panel so that either filter may be placed over the CRT while the other is stowed.

The present day filter configuration is used as the implosion shield for the CRT. During removal and replacement of either filter in field operation, the CRT face plate must be covered by a shield. Therefore if two filters are necessary, Kaiser proposes to bond an implosion shield directly to the CRT. This protection method is used on the existing VDI.

1.7.5 Reliability Demonstration Test (RDT)

1.7.5.1 GENERAL. RDT tests were conducted in accordance with paragraph 4.4.2.3 of the equipment specification. Complete details are presented in Kaiser Report ETR-77-03, 23 February 1977, submitted separately as Data Item Requirement A015, 2nd line, Item 0003. Originals of the complete RDT test logs, brief operational test data, and all ATP data are stored at the Kaiser facility and are available for review. The following summary identifies the highlights and major milestones of the RDT.

The XJ-1 successfully demonstrated an MTBF in excess of the specified 445 hours.

Two XJ-1 units were subjected to a reliability demonstration test program as specified in the following documents:

Government

MIL-STD-781B	Reliability Tests; Exponential Distribution
MIL-STD-883	Test Methods and Procedures for Microelectronics
MIL-C-83421	Capacitors, Fixed, Plastic Film Dielectric
MIL-S-19500E	Semiconductor Devices, General Specification for
MIL-R-39015B	Resistors, Variables, Wire-Wound

Kaiser

13027 Revision B	Reliability Demonstration Test Procedure
ETR-76-04	A6 HRD Failure Rate Prediction

The test program was conducted at Kaiser's Palo Alto environmental laboratory starting July 1976, and successfully concluding on 10 December 1976. Two systems, serial numbers 003 and 004, were tested in accordance with Kaiser RDT Test Procedure No. 13027, Revision B. Test levels were performed in accordance with MIL-STD-781, Test Plan XIX, Test Level E, with a modified low temperature of -30^{o}C; this plan establishes a test-pass criteria of nine or fewer relevant failures in a minimum test time of 2759 hours (6.2 MTBF's). The two systems experienced a total of three relevant failures while accumulating a total of 2772 RDT credit hours, of which 224 hours are ATP time and considered valid RDT credit time in accordance with Paragraph 1.7 g (3) of RDT Procedure 13027. Figure 1-48 shows a typical environmental cycle. Table 1-13 depicts the overall test program and key milestones. Table 1-14 is a chronological log of maintenance actions.

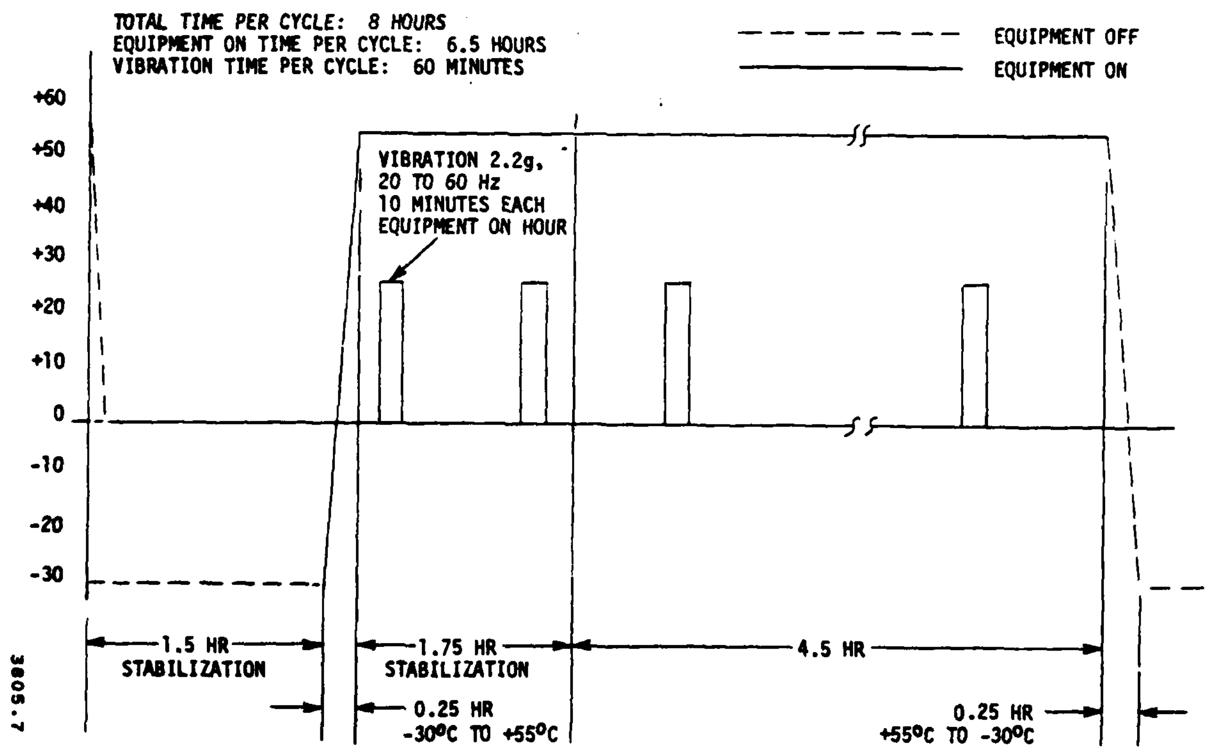


Figure 1-48. One RDT Environmental Cycle

Table 1-13. RDT Test Program Summary

SYSTEM S/N	HOURS AT FAILURE	RELEVANT FAILURES	TOTAL RDT CYCLES	CHAMBER TIME (HRS)	ATP TIME (HRS)
003	202	Feed-Thru Capacitor	177	1150.5	96
004	78 390	Diode, 1N4454 CRH Capacitor	215	1397.5	128
	TOTALS	3	392	2548	224

1.7.5.2 FAILURE SUMMARY. Table 1-15 summarizes failure events in chronological order. The three relevant failures were considered random in nature and no corrective design action was deemed necessary. Detailed failure analyses are contained in Appendices A, B, and C of Kaiser report ETR-77-03.

1.7.5.3 RELIABILITY TEST SUMMARY. Figure 1-49 is a plot of relevant RDT failures versus time and the accept/reject criteria of Test Plan XIX of MIL-STD-781B. The equipment achieved 2772 RDT credit hours with only three relevant failures. Analysis of the data allows the following conclusions:

- The XJ-1 exhibited an MTBF of 759 hours to the 50% confidence level assuming a constant failure rate.
- The XJ-1 exhibited an MTBF of 1100 hours using a Duane growth model.
- The XJ-1 exhibited an MTBUMA of 208 hours using a Duane growth model.

The following paragraphs provide supporting calculations and details for the above conclusions.

Table 1-14. Elapsed Time to Maintenance Action (ETM Readings) From Initiation of RDT

VDI SN	FAILURE DATE	TOTAL TIME IN TEST (ETM READING)			CUM MAINT ACTIONS	TIME CUM MA
		SN 3	SN 4	TOTAL		
3 & 4	7/14	--	--	--	0	--
4	7/15	--	--	--	0	--
4	7/17	66	26	92	1	92
3	7/17	66	26	92	2	46
3	7/24	91	26	117	3	39
3	7/28	106.5	78.5	185	4	46
3	7/28	--	--	--	-	--
3	7/28	109.5	81	190.5	5	38
3	8/5	--	--	--	-	--
4	8/6	137	119	256	6	43
4	8/19	138	123	261	7	37
4	8/26	139	238	277	8	34
3	9/14	--	--	--	-	--
4	9/14	275	311	586	9	65
4	9/15	--	--	--	-	--
4	9/15	288	321	609	10	61
3	9/15	288	321	609	11	55
3	9/16	302	334	636	12	58
4	9/17	308	360	668	13	51
3	9/21	373	425	798	14	57
4	9/28	469	550	1014	15	68
3	10/2	550.5	654	1204.5	16	75
4	10/2	550.5	654	1204.5	17	71
4	10/3	--	--	--	--	--
3	10/5	603	685	1288	18	72
3	10/16	826	865	1691	19	89
3	10/24	--	--	--	--	--
3	10/31	968	1237	2205	20	110
4	11/2	968	1370	2338	21	111
4	11/3	--	--	--	--	--
4	11/3	968	1399	2367	22	108
4	11/21	--	--	--	--	--
TEST FINISH	--	1748	1894	3373	22	153

-- indicates censored data

Table 1-15. Summary of Relevant Failures

SN	DATE/TIME OF FAILURE	FAILURE SYMPTOM	RDT HOURS	TFR REPORT	PART LOCATION	PART TYPE (MFR)	ANALYSIS
003	9/21/76 1500 (+55^{o}C) ETM 540	lost display	202.0	29362	LVPS FL2	ceramic feed-through capacitor (AVS)	Failure of this capacitor (KAE P/N PC 77030-3) resulted in loss of ±30V. Subsequent exam indicated 130Ω short, case to terminals. Sectioning revealed damaged dielectric material. Prior to going completely short, the dielectric exhibited a semiconductor effect. The material does not appear to have been necessarily over-stressed, but defective. (See CER 2121).
004	7/17/76 2130 (+55^{o}C) ETM 128	INS Fail-safe inoperative	72.8	28319	Video amp (CR-20)	JTX 1N4454 (T.I.)	Failure found to be an intermittent diode. Exerting very slight axial pressure (≈ 3 grams) would cause diode to function normally. This diode junction was not a metallurgical bond with only slight evidence of bonding material remaining on the mounting post.
004	10/2/76 0105 (25^{o}C) ETM 756	loss of flite path	390	24366	Board 7 (C8)	CRH Style (CRC)	During the conduct of the scheduled 90th cycle ATP, the flite path disappeared. The problem was traced to C8 in Board 7. Suspect end termination opened. (See CER No. 2120).

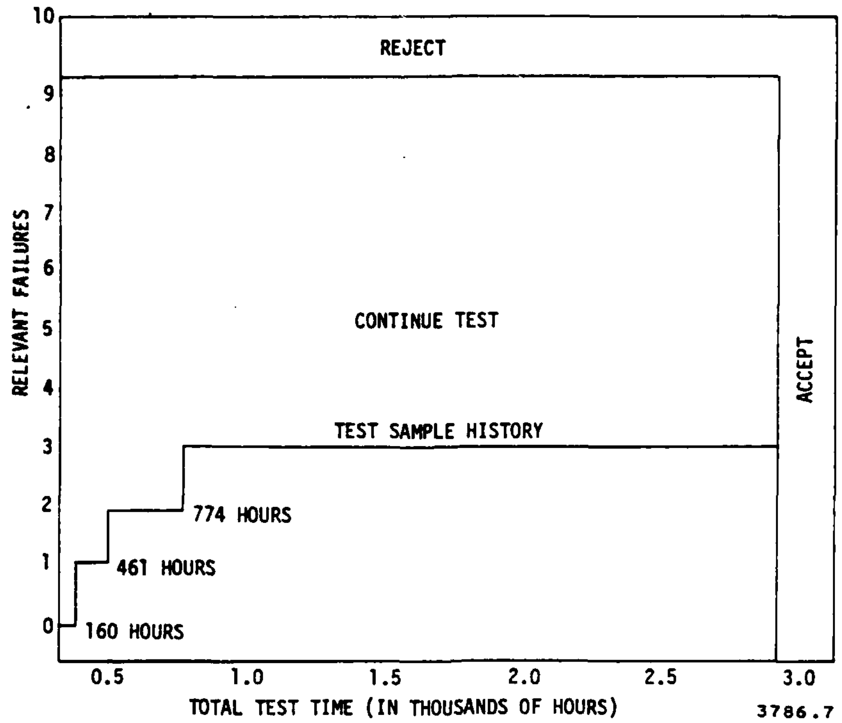


Figure 1-49. Test Plan Criteria

a. Constant Failure Rate Model

The MTBF to the upper 50% confidence interval is defined by the following equation:

$$\text{MTBF} = \frac{2T}{X^2{}_{2K+2;0.5}} = \frac{2X2772}{7.344} = 759 \text{ hours.}$$

where:

T = Total Test Time = 2772 hours

K = Quantity of relevant failures = 3

X^2 = chi square value = 7.344 with K = 3

b. Duane Growth Model for MTBF

The Duane growth model was prepared using the relevant failure incidents and a fourth data point obtained by assuming an additional failure at the test conclusion. Figure 1-50 is a plot of the data points on log-log paper showing a growth rate (α) of 0.475. This data shows that the XJ-1 design has a current MTBF of 1100 hours.

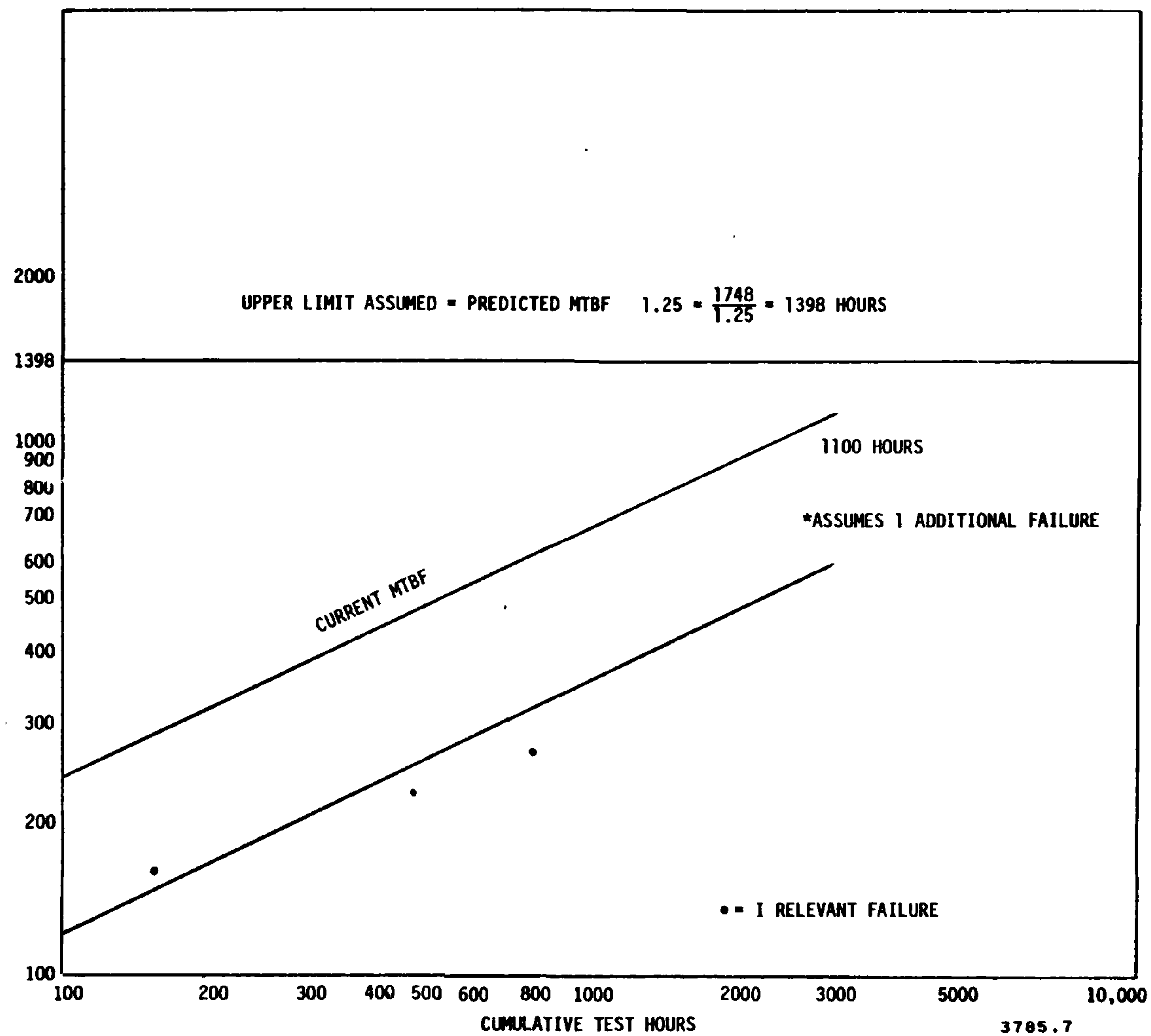


Figure 1-50. Duane Growth Model

The assumption of an additional failure at the 2772 hour point is a conservative assumption, but is warranted because of the paucity of data points on this plot.

c. Duane Growth Model for MTBUMA

Among the most useful life cycle cost data to be obtained from the test data and failures is an estimate of the inherent mean-time-between-unscheduled-maintenance actions (MTBUMA) (figure 1-51). The data presented here includes all failure incidents except those that would not exist in a typical aircraft installation. This plot included all relevant failure incidents, wear-out failures, repair (maintenance) errors, and unconfirmed intermittents. Excluded from the data are those incidents that involved:

1). Environmental conditions beyond those anticipated in the aircraft.

2). Test equipment malfunctions or test operator errors. Since test equipment will not be used at organizational maintenance levels, these incidents should not impact the MTBUMA.

3). Multiple failures discovered during a single maintenance action. These incidents were documented on separate reports but were counted as single maintenance action in the analysis of the data.

This plot differs from the previous data in that the time scale is based on ETM readings and includes operating time during troubleshooting, RDT verification cycles, and time excluded from the official RDT because of various bookkeeping rules of the demonstration test. Table 1-14 was used to plot the MTBUMA Duane plot. This data plotted on figure 1-51 shows the MTBUMA of the design is presently 208 hours and can be expected to grow to approximately 313 hours as mature production systems are deployed to the field.

1.7.5.4 RELIABILITY DESIGN DATA. The XJ-1 design is the result of an intensive reliability effort including:

- Maximum utilization of standard electronic components (M38510, JTX, and ER devices)
- Non-standard parts approval of the relatively few non-standard parts required
- Detailed analysis of component stress levels against severe derating constraints
- Prediction of part failure rates per MIL-HDBK-217B
- Thermal analysis
- FMEA analysis

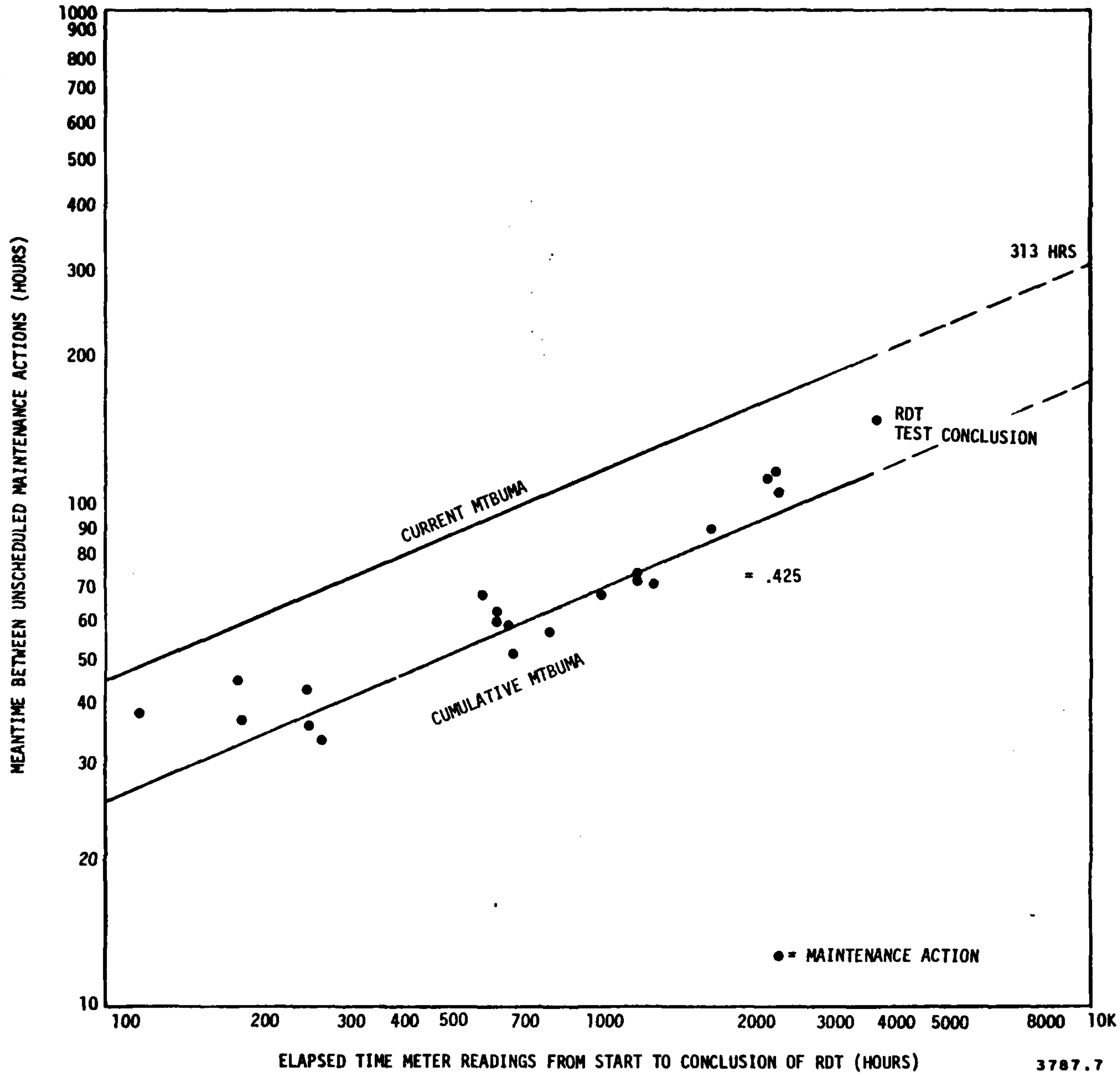


Figure 1-51. Meantime Between Unscheduled Maintenance Actions (MTBUMA) Duane Plot Based on RDT Data

The mature production system MTBF as calculated during the development program was 1748 hours. Details of the MTBF prediction are contained in Kaiser report ETR-76-04, A6 HRD Failure Rate Prediction.

1.7.5.5 CONCLUSIONS. The XJ-1 successfully demonstrated a specified MTBF of 445 hours, and a minimum acceptable MTBF of 222.5 hours.

It must be realized that the systems used to demonstrate the MTBF must be regarded as preproduction systems, and the mature production systems will achieve MTBF's in excess of that presently established. Although the components used in the RDT systems are identical to the components that will be used in production, the printed wiring boards in the RDT systems have been subjected to extensive rework and jumper wiring that will not exist in the production hardware. The mature production system SRA's will therefore be constructed to superior workmanship standards and be subjected to less rework. It is logical to anticipate a significant reliability growth for the production system because of the reduction of severe rework stress on components and the elimination of jumper wiring. The Duane growth models show that the mature production systems can reasonably be expected to achieve field MTBF's in excess of 1100 hours and the filld mean-time-between-unscheduled-maintenance-actions (including wear-out failures) will exceed 300 hours early in the production program.

1.7.6 Qualification Test Summary

1.7.6.1 GENERAL. Qualification test were conducted in accordance with paragraph 4.3.3.2 of the equipment specification, as listed in table 1-16, and Kaiser document 13022, Qualification Test Procedure.

On 1 August 1977 Kaiser successfully completed the qualification test program for the XJ-1. Qualification testing initially utilized SN 002. Upon completion of RDT, SN 004 was utilized to complete certain portions of the qualification tests. The qualification test report, Kaiser Document 13199 Data Item A013, was submitted to NAVAIR on 18 October 1977.

Upon completion of the qualification test program, SN 002 and SN 004 were functional. SN 003 was cannibalized for parts and will require substantial engineering and rework to function normally.

Included in the following summary is an identification of all qualification tests performed and problems which were unique to specific tests, as well as corrective action/design changes which will be incorporated in the production design as a direct result of qualification testing.

1.7.6.2 QUALIFICATION TEST REVIEW. The following paragraphs deal with those portions of the qualification test that required corrective action and design changes.

1.7.6.3 EMI. EMI testing was conducted on SN 002 with minor deviations noted. A deviation request was submitted to the Navy and approved. The EMI Test Report Data Item A014 was submitted to NAVAIR and approved in the summer of 1976.

1.7.6.4 HUMIDITY. The humidity test was completed before the salt fog test. Corrective action and/or design changes from unsuccessful salt fog tests were incorporated prior to the final humidity test. The corrective action and/or design changes which were the direct result of the humidity testing are outlined below.

- The LVPS capacitor module assembly, PN 32140, required conformal coating.

- Excessive moisture was getting under components on printed wiring boards, especially integrated circuits, causing display problems. Initially, conformal coating was poured or sprayed on the boards. This method of applying coating was found to be inadequate. Most of the boards were subsequently dipped into the potting compound to pass the test. As corrective action for production, all boards will be dip potted; this change will be reflected on the production drawings.

Table 1-16. Qualification Test Summary

QUALIFICATION TEST	COMPLETION DATE	SYSTEM SN	CORRECTIVE ACTION OR DESIGN CHANGE
1. Crash Safety Shock	21 April 1976	Mock-Up Unit	None
2. Power Characteristics	13 May 1976	SN 002	None
3. Acceleration	17 June 1976	SN 002	None
4. EMI	10 July 1976	SN 002	Requested Deviation to Specification
5. Cooling Performance	19 July 1976	SN 002	None
6. Design Mechanical Shock	1[illegible] August 1976	SN 002	None
7. Sand & Dust	26 August 1976	SN 002	None
8. Explosive Atmosphere	30 August 1976	SN 002	None
9. Explosive Decompression	1 October 1976	SN 002	None
10. Humidity	22 April 1977	SN 004	Yes
11. Temperature Shock	28 April 1977	SN 002	None
12. Salt Fog	2 May 1977	SN 004	Yes
13. Micra-Interchange-ability	27 May 1977	SN 002	None
14. SACE/Mini SACE Compatibility	22 June 1977	SN 002	None
15. Temperature/Altitude	28 June 1977	SN 004	Yes
16. Vibration	1 August 1977	SN 002	Yes

• During the post-humidity test BOT the roll servo was inoperable. The anti-backlash gear was mounted too close to the board. For production units, the roll servo PWB will be reconfigured. Drawing 32310 documents this change.

1.7.6.5 SALT FOG. The most subtle problem during salt fog test was caused by the system I/O connectors. These connectors were selected originally because they were the solder type and took up less volume. However, these connectors were not environmentally sealed, and are believed to have contributed to five failures in five attempts. For the final salt fog test, the connectors were sealed with epoxy. For production, Kaiser will use environmentally sealed crimp style connectors; this is the same connector used on the old ADI. Kaiser drawing 32113 defines the details for the connector change.

During one of the salt fog tests it was observed that water was not draining out of the box. Holes were drilled in the unit to allow proper drainage. The following Kaiser drawings define changes which correct this deficiency and which will be incorporated in the production design.

32262
32112
32246

On three occasions the flex cable failed. This cable, Kaiser PN 32137-1, connects the front end of the unit to the motherboard. Due to the poor reliability of the cable, it was replaced with a harness. Kaiser drawing 32136 defines the new harness. To facilitate installation of the harness, the casting was modified as shown in Kaiser drawing 32112.

Several problems occurred during salt fog testing with respect to connector and harness connections at the motherboard. Clear RTV (3140) was used where feasible to seal those connections. Sealing was essential for the LVPS connector, I/O interface with the motherboard, line scan harness, front end harness, video amplifier harness, and the high voltage harness. Conformal coating was injected with a syringe between the rest of the connectors and the motherboard. This sealing process will be incorporated into the production units. At the time when the new documentation is generated, the sealing process will be added to the respective drawings.

1.7.6.6 TEMPERATURE/ALTITUDE. The design deficiencies uncovered during this test were as follows: The AH0140 analog switches fail to switch at cold turn-on, the roll servo assembly failed to roll acceptably at cold turn-on, and the line scan phase lock loop did not lock at cold temperature.

Correcting the analog switch problem required designing a circuit which was added to the field scan board #1. This new circuit pulses all the analog switches at turn-on. The drawings listed below document changes that were made.

Drawing	Revision
32172	A
32171	A
32190	F
32380	C
32011	F

Drawing	Revision
32010	G
32071	H
32070	J
32081	C

Mechanical rotational problems were experienced with the roll servo. A consultant was brought in to solve the problem. Also, Singer Kearfott Co. lent support. Singer Kearfott determined that the lubricant used in the motor PS77025 could cause problems at -54^{o}. Singer Kearfott recommends the use of the Braycote lubricant 3L-38RP in the motor. This will require a change in the procurement drawing. Although this new lube was not utilized in the test, Kaiser will use it in production. As result of the roll servo investigation, it was determined that the motor gear had the wrong pitch. The correct gear was obtained and used in the test. Kaiser drawing 32264 documents the gear change. Rusting of the bearings was discovered during testing and will be corrected by the use of stainless steel bearings in production. The flaking rust particles identified a potential interference problem between one of the roll servo bearings and the slip ring assembly. Kaiser drawing PS83506 documents the change which was made to the slip ring assembly to relieve interference. After doing the above, the roll servo no longer exhibited operational deficiencies of environmental extremes.

The phase lock loop has historically been a problem at cold temperature. An exhaustive engineering effort was made in May, 1977 to resolve the locking problem at cold temperature. Kaiser drawings 37172, revision E, and 32380, revision B, document the design changes to the line scan phase lock loop. These design changes have stabilized the operation of the phase lock loop over the specified temperature range.

1.7.6.7 VIBRATION. *Vibration testing at 5g was by far the most* difficult test for the XJ-1 to pass. During the course of this test it became necessary to utilize several components and boards from VDI SN 003. Many minor failures could be attributed to the prototype nature of the equipment, such as broken leads on piggy-back components.

While vibration testing was being done on the unit in the longitudinal axis, it was observed that the symbol generator boards would not remain seated. The rear top cover was redesigned so as to insure that the boards would remain seated. The following Kaiser drawings document the rear top cover design change.

Drawing	Revision
32244	E
32477	-
32577	-

Also, during this portion of the test it was observed that roll servo motor clamp 32266-1 was not adequately restraining the motor. Kaiser drawing 32266, revision B illustrates the design change that corrected this problem.

The lateral axis of vibration caused the greatest destruction to the unit. In this axis the symbol generator boards experienced maximum displacement, causing boards to become intermittent and components to break. It was determined that most synchro-to-digital hybrid components manufactured by ILC/DDC corporation before 1975 could fail in vibration. Several of these hybrids failed as different boards were substituted into the system. Newly manufactured hybrids from DDC were required to complete vibration testing.

Board vibration displacement was reduced by extending the card guides down closer to the motherboard, the addition of snubbers on the symbol generator boards, and the simulation of narrower card guides by utilizing mylar tape along the edges of the boards. Because of the jumper wires on the boards, board snubbers were used instead of stiffeners. Board stiffeners will be used in production. The stiffener locations will be a function of the new board layouts.

Kaiser drawing 32111, revision E, documents the design change to the rear chassis that extends and narrows the card guides.

The vertical axis vibration test uncovered two problems. The front top cover of the system would "oil can" severely during vibration. The display would lose sync as a result of chattering relays on the video amp.

It was determined that it was necessary to stiffen the top cover to minimize the oil can effect. For the test, a metal "X" brace was bonded to the cover. This reduced the oil can effect substantially. Because of space requirements the top cover will be embossed on production units. The embossed cover will be of equivalent strength to the test cover and is documented in Kaiser drawing 32232.

The video mode relays are mounted to the video amplifier board which is mounted to the front top cover. The relays still chattered with the added cover support. For the test, the relays were removed from the video amp and video mode switching was effected external to the unit. Once the relays were removed, the vertical axis vibration was completed with no problems. The relays are currently being designed out of the system. In lieu of relays, video switching will be accomplished electronically.

1.7.7 Flightworthiness Test

1.7.7.1 GENERAL. The following paragraphs present the detailed results for the crash safety test necessary for flightworthiness qualification. Qualification consisted of verifying the applicable requirements specified in Design Requirements document 32591.

1.7.7.2 PURPOSE. The crash safety test was performed to demonstrate that the XJ-1 can withstand the expected dynamic crash shock stresses and not create a hazard.

1.7.7.3 APPLICABLE DOCUMENTS. The following documents are applicable to the tests.

MIL-T-5422F, Paragraph 4.3.2.2
Design Requirements Specification 32591
Qualification Test Procedure 13022.

1.7.7.4 STANDARD CONDITIONS. The following environmental conditions prevailed during test conditions.

- Room ambient temperature of 22°C.
- Ambient atmosphere pressure of 29.98 inches of mercury.
- Ambient humidity of 44% R.H.

1.7.7.5 FACILITIES. The test was conducted at the Lockheed Missile and Space Division Facility, Sunnyvale, California.

1.7.7.6 WITNESSING/CERTIFICATION. The test was directed by a KE test engineer and witnessed by a KE quality control representative, to assure that all applicable portions of the quality program plan were implemented during test conduction. An AFQAR representative witnessed the test.

1.7.7.7 PROCEDURE AND RESULTS. The mock-up was attached by normal mounting provisions to a test fixture and the test fixture installed on a shock machine. The mock-up was subjected to two shocks in each direction, along three mutually perpendicular axes, for a total of 12 shocks in accordance with paragraph 4.6 of Qualification Test Procedure 13022. Each shock pulse had nominal peak value of 30g, and a nominal duration of 11 milliseconds. After the second shock pulse was applied in each axis, the mock-up was removed and a visual inspection was performed, verifying that no deleterious effect had occurred.

1.7.8 Production

1.7.8.1 GENERAL. The following paragraphs discuss various subjects related to production of the XJ-1, in particular:

- Drawing status
- Tooling
- Long-lead items
- Facilities

1.7.8.2 · DRAWING STATUS. Present system drawings will not be sufficient for production. Most drawings can be classified as engineering drawings, i.e., not suitable for defining a production configuration. Many changes made to the system have been documented but not incorporated into the drawings. Funds for generating production drawings will be allocated by the Navy upon the initialization of a production contract.

1.7.8.3 TOOLING. Kaiser has the following tooling available for XJ-1 production.

1 Mill Fixture
1 Mill Fixture (4 Surfaces)
5 Drill Fixtures
2 Holding Fixtures
1 Holding Fixture (Drill Template)
1 Casting Die (Strain Relief Bkt.)
Side Panel Drill Jig
CRT Assembly Fixture
Wire Harness Jig
Deflection Heatsink Jig
Deflection Heatsink Bending Rail
Deflection Heatsink Masterplate
Deflection Bending Rail
Clamp for HV Wire, Fixture

Clamp for HV Wire, Jig
CRT Housing, Cut Jig
CRT Housing, Drill Jig
Frame Filter Jig
Chassis Cut Jig
Tray Assembly, Fixture
Tray Assembly, Jig
Tray Assembly, Template
Tray Assembly, Press Tool
Tray Assembly, Masterplate
Tray Assembly, Bending Rail
Tray Assembly, Press Tool
Air Flow Valve, Jig
Cap Valve, Casting Die
Housing, Casting Die
Air Flow Valve, Casting Die
Plunger Gasket Die
Cap Gasket Die
Ring Gasket Die
Seal Plunger Die

1.7.8.4 LONG-LEAD ITEMS. Long-lead categories for the XJ-1 are as follows:

- Castings, 8 per system
- Mechanical parts, 8 items per system
- Electro-mechanical, 7 items per system
- Transformers, 8 items per system
- Printed wiring boards, 23 per system
- Electronic components, i.e. capacitors, CRT, yoke, A/D converter, 3-phase bridge

Casting lead time can be up to 12 weeks after which machining and other processing must be accomplished, giving a total lead time before assembly up to 24 weeks.

Electro-mechanical parts such as connectors have lead times of 12 weeks.

Transformer lead time can be 10 weeks to 12 weeks.

Printed wiring boards can have lead times as long as 14 weeks.

Electronic components have lead times up to 20 weeks. Capacitors may have even longer lead times due to upheavals in that industry that have recently occurred due to foreign competition.

1.7.8.5 FACILITIES. The following facilities are available for XJ-1 production.

PLANT I - 32,000 square feet
PLANT II - 73,000 square feet

MANUFACTURING - 2/3 of 1 shift (days)

	CAPACITY	UTILIZATION
EXAMPLES -		
Electro/mechanical	23 stations	14 working
P.C. Board	42	30
Harness	27	17
Push Line	16	4 (part time)

AREAS REQUIRING ADDITIONAL FACILITIES

Environmental Chambers - space available
Special Test Equipment - space available

1.7.9 Weight Control

The design requirements specify that the equipment shall not weigh in excess of 45 pounds. Utilizing durable investment castings, the weight of the unit was kept down while the structural integrity was improved with respect to the original system. The average weight of the XJ-1 is 43 pounds. This weight should remain almost unchanged for production as new circuits will be added but most of the extraneous wires will be removed.

1.7.10 Conclusions

The prototype XJ-1 demonstrated a mean-time-between-failure of 759 hours, significantly in excess of specification requirements.

Modular design, functional partitioning, built-in test and accessible SRA test points insure easier maintenance, at lower skill levels, than the presently deployed ADI. A 55 minute MTTR has been demonstrated.

The XJ-1 simplifies logistics by using modern parts that are more easily obtainable than those in the ADI.

Users have expressed general satisfaction with the XJ-1. Deficiencies noted during flight test have been corrected or have been analyzed in sufficient detail to permit rapid correction prior to initiation of production.

PART II

RECOMMENDATIONS

As a result of the extended period of time for which this program has been in the preproduction, many new display components have come into existence that will improve the operation and reliability/maintainability of this system.

In the area of synchro-to-digital hybridized circuits, vendors have reduced the quantity of components required to do the same function thereby improving reliability.

High voltage power supplies are being manufactured presently which are more efficient, smaller, significantly lighter, and at minimum function with the same performance levels.

Because of the fast-growing display technology and demands, high voltage focus CRT's are finding their way into airborne display systems. These CRT's allow for increased anode voltage which thereby increases the light output while maintaining high resolution.

Therefore, it is recommended that the above items be investigated for possible use in the production phase of the A6 XJ-1 Display Program.

PART III

SUPPLEMENTARY DATA

The following data items were submitted to the contracting agency during the term of the contract.

Data Item	Title	Date Submitted
A001	Non-Standard Parts, Materials, & Non-Repairable Subassys.	9 April 1976
A002	Microelectronic Devices & Assys.	10 April 1975
A004	Cooling Design Data	8 January 1976
A006	Maintainability & Support Equipment Report	12 January 1976
A007	Interference Compatibility Test Plan	5 January 1975
A008	Reliability Program Plan	April 1975
A009	Acceptance Test Procedure	5 January 1975
A010	Acceptance Test Results	14 July 1977
A011	Progress Report Letters	Monthly
A012	Qualification Test Procedure	27 January 1976
A013	Qualification Test Results	18 October 1977
A014	EMI Test Report	8 November 1976
A015	Reliability Test Reports	8 March 1977

FILMED

8 - 8

DTIC